

# Technical Program

1:00pm-1:15pm **Welcome and introduction to workshop**

1:15pm-2:45pm **Optimizations**

**Length Adaptive Processors: A Solution for the Energy/Performance Dilemma in Embedded Systems**

Balaji V. Iyer, Jesse G. Beu, Thomas M. Conte (Georgia Institute of Technology)

**ArchExplorer.org: Joint Compiler/Hardware Exploration for Fair Comparison of Architectures**

Veerle Desmet (Ghent University, Belgium), Sylvain Girbal (INRIA Saclay & Thales Research, France), Olivier Temam (INRIA Saclay, France)

**Elastic-Hyperblock: A Power Aware Hyperblock Structure**

Muhammad Umar Farooq, Lizy K. John (University of Texas at Austin)

3:30pm-5:00pm **Memory Systems**

**Coherence Miss Classification for Performance Debugging in MultiCore Processors**

Guru Venkataramani (Georgia Institute of Technology), Christopher J. Hughes (Intel Corp), Sanjeev Kumar (Facebook Inc), Milos Prvulovic (Georgia Institute of Technology)

**Automatic Adaptation of Transactional Memory State Management to Application Conflict Patterns**

Daniel Lupei, Adam Czajkowski, Cedomir Segulja, Michael Stumm, Cristiana Amza (University of Toronto)

**Instructing the Memory Hierarchy with In-Cache Computations**

Patrick A. La Fratta, Peter M. Kogge (University of Notre Dame)