CS/COE 0447 Fall 2009
Lab 12: Splitters and Combinational Analysis Tool
Due Date: December 10, 2009

To get started on this lab, attend recitation on 12/04. Each of you should submit your own solution, according to these instructions: http://www.cs.pitt.edu/~sab104/teaching/cs447/submission.html. You may collaborate with your partner, but each person must turn in their own copy of the lab, with the name of their partner. The lab is due on 12/10 at 11:59pm.

For this lab, we will use a tool for designing and simulating digital circuits. The tool is called *Logisim* and is available at http://ozark.hendrix.edu/~burch/logisim/.

1) Parity Generator

A parity bit is an extra signal that is added to a data word to enable error checking. An *even* parity bit is 1 when the data contains an even number of ones. An *odd* parity bit is 1 when the data contains an odd number of ones. For example, the even parity of the binary number 01100110b is 1 and the odd parity of the number 10011101b is 1.

A parity generator is a logic circuit that generates the parity bit of a data word. Your task is to build a parity generator for a 5-bit word. Your parity generator should generate the even as well as the odd parity. Use the circuit file at http://www.cs.pitt.edu/~sab104/teaching/cs447/labs/parity.circ as a template.

Hint: use the splitter element to separate the individual bits of the 5-bit input.

Hint: use the Combinational Analysis Tool (Window menu) to generate the circuit from a truth table.