Curriculum Vitae

Michael Moeng

Department of Computer Science
University of Pittsburgh
Pittsburgh, PA, 15260
Phone: (510) 684-7416
moeng@cs.pitt.edu
http://www.cs.pitt.edu/~moeng

Research Interest

Computer Architecture: with a focus in the area of Parallel Architecture Simulation Techniques. My advisors are Sangyeun Cho and Rami Melhem.

Education

Ongoing: Ph.D. in Computer Science, University of Pittsburgh, 2007-present
GPA (at start of Spring '10 term): 3.846

B.S. in Computer Science, University of California at Berkeley, 2003-2007
GPA: 3.457

Experience

- Graduate Student Instructor — Spring 2010
  CS2750: Machine Learning, taught by Milos Hauskrecht
  http://www.cs.pitt.edu/~milos/courses/cs2750/
- Graduate Student Instructor — Fall 2010
  CS1541: Undergraduate Computer Architecture, taught by Rami Melhem
  http://www.cs.pitt.edu/~melhem/courses/1541p/index.html
  CS2410: Graduate Computer Architecture, taught by Sangyeun Cho
  http://www.cs.pitt.edu/~cho/cs2410/
- Graduate Student Instructor — Spring 2010
  CS1550: Intro to Operating Systems, taught by Jonathan Misurda
  http://www.cs.pitt.edu/~jmisurda/teaching/cs1550.htm
  CS2750: Machine Learning, taught by Milos Hauskrecht
  http://www.cs.pitt.edu/~milos/courses/cs2750/
- Graduate Student Instructor — Summer 2008
  CS131: Software for Personal Computing, course web page at
  http://www.cs.pitt.edu/~moeng/cs131.html
  University of Pittsburgh, Department of Computer Science

Awards

- A&S Graduate Fellowship, University of Pittsburgh, Fall 2007 and Spring 2008
- Undergraduate Student Award for excellent project work in CS152 (Undergraduate Computer Architecture) , University of California at Berkeley, May 2007

Research Projects

- Parallel Simulation Techniques — Started Spring 2010
  Exploring simulation on multicore hosts or using co-processors
- Energy Management Using Learned Inter-core Interactions — Started Summer 08
  Applies statistical machine learning techniques to multicore chips with Dynamic Voltage/Frequency Scaling (DVFS) capability. The goal is to improve chip-wide energy-efficiency with a trained policy that has low runtime overhead.
- Two-Phase Trace-Driven Simulation(TPTS) — Started Fall 2007
  TPTS is a framework for fast multi/many-core simulation by breaking simulation into functional and timing portions. The cost of functional simulation is paid once by creating a trace of important events. This cost is then amortized over multiple timing runs which alter architectural parameters.

Publications

- Michael Moeng, Rami Melhem. **Applying Statistical Machine Learning to Multi-core Voltage & Frequency Scaling**. Computing Frontiers, pp. 277~286 , May 2010.
- Hyunjin Lee, Lei Jin, Kiyeon Lee, Socrates Demetriades, Michael Moeng, and Sangyeun Cho. **Two-Phase Trace-driven Simulation (TPTS): A fast multicore processor architecture simulation approach**. Software: Practice and Experience (SPE), 40(3): pp. 239~258, March 2010.
- Sangyeun Cho, Michael Moeng, and Rami Melhem, **Energy Corollaries to Amdahl's Law**, Microprocessor Report (MPR), October 2008.
- Sangyeun Cho, Socrates Demetriades, Shayne Evans, Lei Jin, Hyunjin Lee, Kiyeon Lee, and Michael Moeng, **TPTS: A Novel Framework for Very Fast Manycore Processor Architecture Simulation**, Proceedings of the Int'l Conference on Parallel Processing (ICPP), pp. 446~453, Portland, Oregon, September 2008.