

Michel Hanna

Contact Information

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Research Interests

1. High-performance routers and switches packet processing engines: packet forwarding, packet filtering (classification) and deep packet inspection (DPI).
2. Energy efficient routers and networked platform architectures.
3. Set associative (content addressable) memory architectures (e.g., TCAM).
4. Efficient hashing, tree and trie algorithms for hardware implementation.
5. Network security.

Education

08/2005 – (expected December 2011) University of Pittsburgh, PA, USA
Ph.D. Candidate, Computer Engineering Program, Computer Science Dept.
Thesis Proposal title, “High-Performance and Scalable Packet Processing Engines Using Set Associative Memory Architectures”.

11/16/2009 University of Pittsburgh, PA, USA
M.S. in Computer Engineering
Thesis title, “Advanced Hashing Schemes for Packet Forwarding using Set Associative Memory Architectures”

09/1999 - 12/2004 Cairo University, Cairo, Egypt
M.S. in Electrical Engineering
Thesis title, “Real Time Analysis of FIP-Based Systems”

09/1994 – 07/1999 Cairo University at Fayoum, Fayoum, Egypt
B.S. in Electronics and Electrical Communications Engineering

Work Experience

03/2011 – 09/2011 Huawei (Futurewei) Technologies, Santa Clara, CA, USA
System Architect Intern for Smart Memory NP

- I am working on the architecture of the next two generations NP chips from Huawei. The first generation processor will achieve 100Gbps while covering wide range of packet processing applications: forwarding, classification, deep inspection, accounting, etc. I participated in designing the memory address translation units and I wrote their RTL code. Also, I participated in reviewing the macro and micro arch of the main components of this chip.
- I am the principle architect of the packet classification engine for the second generation NP. This includes the high level mapping of one of the fastest software packet classification algorithms to this chip hardware platform, writing the macro and micro arch documentations, participating in the RTL coding of some units of this engine, and I helped designing the network on chip (NoC) for this chip as well. In addition, I helped optimizing the native

algorithm prior mapping it via the use of C/C++ simulation. This second generation will provide between 300PPS and 600PPS throughput.

- In addition, I am filing two patents with my teammates, one for memory address translation and one for packet classification.

09/2006–12/2006 *Bosch RTC , Pittsburgh, PA, USA*

Computer Networks (Fieldbus) & Middleware Research Intern

- Designed and implemented a multithreaded C++ **Controller Area Network**-based (CAN) transmission protocol inside Bosch's middleware environment "MIDAS". We successfully tested our system using a test-bed.

02/2007- Now *University of Pittsburgh, PA, USA*

Research Assistant, Computer Science Department. CA-RAM Project

- Developed novel memory architecture, Content Addressable RAM or CA-RAM, with 70% lower power consumption and 45% lower space than the widely used Ternary Content Addressable Memory (TCAM). I developed novel hashing (plus other hash aiding techniques) schemes to store an entire packet engine database (e.g., forwarding table, packet filtering rules) in a single RAM chip. Received an NSF grant in support of this project.
- Currently, my research is extending the use of CA-RAM for deep packet inspection and utilizing new memory technology (e.g., PRAM) to reduce power consumption than the DRAM technology.

09/2005- 09/2006 *University of Pittsburgh, PA, USA*

Research Assistant, CS Department. HPC/PERCS Project

- Helped build accurate trace-driven interconnection network simulator with two networks for high performance multiprocessor super computers. We used MPICH library to emulate the actual model.

09/1999 – 12/ 2004 *Cairo University, Cairo, Egypt*

Research Assistant, Real Time Lab, E.E. Dept. FIP Fieldbus Project

- Developed an analytical model for worst case analysis and real time guarantees of Factory Instrumentation Protocol (FIP). The accuracy of our model was 0.5% from simulation analysis.

Programming Skills, Network Protocols & Simulation tools.

- **Proficient in C and C++:** 11 years working experience in C/C++, 3 years in C++ STL and multithreaded programming (less than a year).
- **Network Protocols:** Very good experience with network programming, multithreaded socket programming, OpenSSL library, Controller Area Network (CAN) transmission protocol implementation and products, Factory Instrumentation Protocol (FIP). Deep understanding of Ethernet, TCP/IP and SDH (SONET) networking protocols.

- **Hardware languages:** I did a couple of projects using Verilog RTL with Huawei. I also taught VHDL using Active VHDL for the ECE undergrads.
- **Good knowledge of x86 assembly language:** Used Intel "x86" assembly language in a couple of projects. In addition, I taught it in a hardware interfacing course for five years.
- **Encryption and Coding:** Very good experience with BCH, CRC's, Reed-Solomon error correcting codes and RSA encryption implementation.
- **Other programming languages:** Good experience and teaching multiple courses with Java. Familiar with scripting languages: Python, Perl and PHP, and MySQL DB.
- **Simulation Tools:** Matlab, Simulink, MPICH2, Active VHDL and CSIM simulation library.
- **Operating Systems:** Unix, Linux, MS Windows.

Teach Experience

Fall 2007, 2008 and 2009 University of Pittsburgh, PA, USA

Teaching Fellow: teaching different undergrad courses on programming languages and introductory level courses for Personal Computing.

09/1999 – 05/2005 Cairo University at Fayoum, Fayoum, Egypt

Teaching Assistant: Electronics and Electrical Communications Engineering Dept. teaching senior level undergrad courses: Computer Architecture, Operating Systems, Data Structures and Algorithms in C/C++ and Java, Computer Networks, Introduction to Programming in C/C++, Introduction to OOP in Java/C++, Microprocessors and Interfacing, Digital and Analog Electronic Circuits, Digital and Analog Communications, Digital Signal Processing.

Honors, Awards and Grants

1. **NSF** Travel Grant to attend IEEE/ACM ANCS 2009.
2. **First on class** and undergrad **Honor** Degree, Electronics and Electrical Comm. Department, School of Engineering, Cairo University, Fayoum, 1999.

Other Experiences

- Member of organizing committee and web chair of the **NSF** Workshop "**Data Intensive Computing**", University of Pitt., Comp. Sci. Dept., July 2009
- **Reviewer** for IEEE Transaction on Parallel and Distributed Systems (TPDS), Springer Telecomm. Sys. Journal, IEE/ACM Trans. On Net. (ToN), HOTi, ICPP, IPDPS, IEEE Infos and IEEE Infocom.

Publications

M.S. Dissertations:

1. "Advanced Hashing Schemes for Packet Forwarding Using Set Associative Memory Architectures", Computer Engineering Program, University of Pittsburgh, November 2009
2. "Real-Time Analysis of FIP-Based Systems", Electrical Engineering Dept. Cairo University, December 2004.

Articles in Refereed Conferences:

3. S. Demetriades, Michel Hanna, S. Cho, and R. Melhem, "An Efficient Hardware-based Multi-hash Scheme for High Speed IP Lookup", HOTi, August 2008.
4. Michel Hanna, S. Demetriades, S. Cho, and R. Melhem, "CHAP: Enabling Efficient Hardware Hash Schemes for IP Lookup", IFIP Networking, May 2009.
5. Michel Hanna, S. Demetriades, S. Cho, and R. Melhem, "Progressive Hashing for Packet Processing Using Set-Associative Memory", IEEE/ACM ANCS, October 2009.
6. Michel Hanna, S. Cho, and R. Melhem, "A Novel Scalable IPv6 Lookup Scheme Using Compressed Pipelined Tries", IFIP Networking, May 2011.
7. Michel Hanna, S. Cho, and R. Melhem, "Dynamic Multi-Matching/Best-Matching Packet Classification Engine Using eDRAM", to be submitted to IPDPS 2012.

Articles in Archived Journals:

8. Michel Hanna, S. Demetriades, S. Cho, and R. Melhem, "Advanced Hashing Schemes for Packet Forwarding Using Set-Associative Memory Architectures", J. Parallel and Distributed Computing (JDPC), January, 2011.
9. Michel Hanna, S. Cho, and R. Melhem, "Matchless IPv4/IPv6 Packet Forwarding Engine Using a New Inter-Node Compression Scheme", submitted to IEEE/ACM Transactions on Networking (ToN), March 2011.
10. Michel Hanna, S. Cho, and R. Melhem, "Dynamic Multi-Matching/Best-Matching Packet Classification Engine Using Content Addressable RAM Architecture", to be submitted to IEEE Trans. on Comp., 2011.

Patents

- 1- "A Device for Memory Mapping and Translation for Arbitrary Number of Memory Units", Sailesh Kumar, Bill Lynch, Joji Philip and Michel Hanna (filed).
- 2- "A Tree-based Scheme for Splitting and Load Balancing Packet Processing Databases Using Special Encoding", Michel Hanna, Chong Zhang, Sailesh Kumar and Joji Philip (in process of filing).

References

1. **Prof. Rami Melhem** University of Pittsburgh, CS dept., Tel: 412-849-1293, email: cho@cs.pitt.edu.
2. **Prof. Sangyeun Cho**, University of Pittsburgh, CS dept., Tel: 412-983-8371, email: cho@cs.pitt.edu.
3. **Prof. Steven Levitan**, University of Pittsburgh, ECE dept., Tel: 412-648-9663, email: levitan@pitt.edu.
4. **Prof. Taieb Znati** University of Pittsburgh, CS dept., Tel: 412-624-8417, email: znati@cs.pitt.edu.
5. **Sailesh Kumar**, PhD, Senior NP Architect, Huawei tech., Santa Clara, CA, USA, Tel: 314-707-7191, email: sailesh.kumar@huawei.com
6. **Bill Lynch**, PhD, tech. VP, Huawei tech., Santa Clara, CA, Tel: 408-930-4599, Email: bill.lynch@huawei.com.
7. **Sameh Gobriel**, PhD, Wireless Research Scientist, Intel, Hillsboro, OR, Tel: 412-589-4525, Email: sameh.gobriel@intel.com.