Quiz (Lecture 7) Your name:

Q1(3 points): Indicate if each of the following statements is true (T) or false (F):

One Page Table is used for all the processes running on a given core	T	F
A TLB miss always results in a page fault	T	F
Some pages in memory contain entries of the page table	T	F
The number of TLB entries is independent of the number of entries in the page table	T	F
Multi-level page tables are needed to deal with multi-level caches	T	F
The physical address always contains fewer bits than the logical address	T	F

Q2 (2 points): Consider an architecture in which the virtual address of a byte is 28 bits long and a maximum physical memory is 1GB. Complete the following assuming a page size of 1 KB.

- The number of entries in the page table of a process is __2^{18}__
- Assuming that 6 auxiliary bits are needed in each table entry (for the valid, dirty and LRU bits), then the maximum size of each page table entry is 6+20=26 bits
- The maximum page table size is $2^{18} * 4 = 2^{20}$ bytes, which can fit in 2^{10} pages.

Will accept $2^{18} * 26 / 8 = 2^{16} * 13$ $2^{6} * 13$

Q3 (3 points): Consider the shown direct mapped TLB for a system with 256 virtual pages and 64 physical pages, where each page contains 16 words.

(a) For each of the following references to virtual word addresses (which ignores the 2-bit byte offset) indicate if the reference will result in a TLB miss or hit, and in case of a TLB hit, find the physical word address.

0010 0011 1001 → TLB miss

1011 1010 1111 → TLB miss

1001 1111 0101 → TLB miss

	valid	tag	Physical page #
0(000)	1	00100	101010
1(001)	1	11100	001100
2(010)	1	10110	010000
3(011)	0		
4(100)	0		
5(101)	1	10111	111001
6(110)	0		
7(111)	1	00111	001110