Quiz (Lecture 5) Your name:

Q1: (3 points) Indicate if each of the following statements is true (T) or false (F)

A block can be in the state "Exclusive" in one cache and "Invalid" in the other caches	T	F
False sharing may occur only if the cache block contains multiple words	T	F
Cache coherence is not needed for instruction caches	T	F
A write miss to an Exclusive block B generates an "invalidate B" on the bus	T	F
No cache coherence protocols are needed in write through caches	T	F
A block is in the Exclusive state when the valid bit = 1 and the dirty bit = 1	T	F

Q2: (4 points) This question assumes that the cache block size = 1 word and that words A and B be mapped to the same index, X, of the two "write back" caches of two processors P1 and P2.

Following the MSI protocol, complete the following table indicating the state of the block at index X after each of the indicated events if, initially, index X has no valid block in the two caches and that A=B=0 in memory. Use I, S and E for Invalid, Shared and Exclusive, respectively.

In addition to the state of the block after each access, you should also show the bus transaction(s) triggered by the access (request to read, request to write, write back, Invalidate)

	In cache of P1	In cache of P2	In memory
	X → (I)	X → (I)	A=0 , B=0
P1 Reads	Request A to read X → A = 0 (S)	X → (I)	A=0 , B=0
P2 writes A=20	X → (I)	Request A to write X → A = 20 (E)	mem supplies A A=0 , B=0
P1 reads A	Request A to read X → A = 20 (S)	Write back A X → A = 20 (S)	A=20 , B=0
P1 reads B	Request B to read X → B = 0 (S)	X → A = 20 (S)	mem supplies B A=20 , B=0
P2 writes B = 30	X → (I)	Request B to write X → B = 30 (E)	mem supplies B A=20 , B=0

Q3: (1 points) In a MSI coherence protocol, when is a cache controller forced to write back a block, B? (Be brief – answers that are more than 30 words will be ignored)

1) When B is exclusive and is evicted to be replaced by another block
2) When B is exclusive and another cache requests B.