Quiz (Lecture 3) Your name:

Q1: Indicate if each of the following statements is true (T) or false (F) – 3 points:

There can be conflict misses in fully associative caches	T	F
A fully associative cache is slower to access than a direct mapped cache	T	F
Larger block sizes always reduces the miss rate	T	F
In pipelined execution, the same instruction cannot cause a cache miss twice	T	F
The LRU block in the sequence 3, 3, 0, 2, 2, 1, 0, 3, 3 is block 1	T	F
Larger block sizes reduces compulsory misses	T	F

Q2: complete the following sentences – 3 points:

A 4-way associative 8Kbyte memory bank with block size of 32 bytes has a total of 256 blocks

A 4-way associative 8Kbyte memory bank with block size of 32 bytes has a total of 64 sets

In an 8-way set associative cache with 64 sets, the number of bits used as index is 6

Q3: Assume a pipeline in which 30% of the instructions access the data memory (data cache). If the hit rate of the instruction cache is 90% and the hit rate of the data cache is also 90% and the miss penalty of either caches is 50 cycles. Compute the CPI of the pipeline assuming that CPI = 3 when the hit rate of the caches is 100% - 2 points.

$$CPI = 3 + 0.1 * 50 + 0.1 * 0.3 * 50 = 3 + 0.13 * 50 = 3 + 6.5 = 9.5$$