

Quiz (Lecture 2)

Your name:

Q1: Indicate if each of the following statements is true (T) or false (F) (2.5 points):

- Accessing a fully associative cache is faster than a direct mapped cache of the same size T F
- The number of blocks in a direct mapped cache should be a power of 2 T F
- The number of bytes in a cache block should be a power of 2 T F
- In the write through policy, data in memory is always consistent with data in cache T F
- The dirty bit is set when a block is read for the first time in the cache T F

Q2: Complete the following sentences (4 points):

Assuming a 32-word, direct mapped, cache with block size = 1 word:

Memory word address 36 is cached in index 4 (in decimal) and its tag is 1 (in decimal)

Memory word address 001101010 is cached in index 01010 (in binary) and its tag is 0011 (in binary)

Assuming a 32-word, direct mapped, cache with block size = 4 word:

Memory word address 36 is cached in block index 1 (in decimal) and its tag is 1 (in decimal) Memory word address 001101010 is cached in block index 010 (binary) and its tag is 0011 (binary)

Q3: In a 32-bits architecture where a byte address is given by 32 bits $b_{31}, b_{30}, \dots, b_1, b_0$, identify the bits that are used for the tag if the cache size is 2Kbyte and the cache block size = 4 words (16 bytes) (1.5 points).

The tag bits are: b_{31} , b_{30} ... , b_{12} , b_{11}

b_{31} b_{30} b_{29} ... b_2 b_1 b_0
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