Quiz (Lecture 1) Your name:

Q1: For each of the following statements, circle the correct choice (or choices if more than one choice applies) (2.5 points)

Cells need to be refreshed in:	DRAM	SRAM	Flash	Disks
Cells ware out in	DRAM	SRAM	Flash	Disks
The unit of data access in disks is a:	byte	word	sector	track
Cache block = multiple word to take advantage of	spatial locality		temporal locality	
A memory rank is composed of multiple		Dims	channels	chips

Q2: complete the following sentences: (2 points)

A 128Kbyte memory bank should be organized as 1024 rows and 128 columns of bytes

The address of a byte in the 32Kbyte bank described above consists of 17 bits, with 10 bits used for row address and 7 bits used for column address

Q3: Assuming a 16-bytes memory composed of 2 banks, each with 4 rows of 2 bytes each (1+1+1.5)

a) Show on the figure below a bank major then column major ordering of the 16 bytes

0	4
1	5
2	6
3	7

Bank 0

8	12
9	13
10	14
11	15

Bank 1

b) Show on the figure below a column major then row major ordering of the 16 bytes

0	8
2	10
4	12
6	14

Bank 0

1	9
3	11
5	13
7	15

Bank 1

c) Assuming that b3 b2 b1 b0 is the 4-bit address of a byte in the memory, which bit(s) is/are used for bank address, row address and column address in the "bank major then column major" ordering?

i. Bank address uses bit(s) b3
ii. Row address uses bit(s) b1 b0
iii. Column address uses bit(s) b2