Question 1

In this question, consider the following series of word addresses:

20, 33, 21, 4, 21, 17, 28, 45, 33

Assuming a 2-way set associative cache with two-word blocks and total size of 16 words, show the content of the cache after each memory reference and indicate whether it is a hit or a miss.

word 20 = block 10 = 4 * 2 + 2
word 33 = block 16 = 4 * 4 + 0
word 21 = block 10 = 4 * 2 + 2
word 4 = block 2 = 4 * 0 + 2
word 17 = block 8 = 4 * 2 + 0
word 28 = block 14 = 4 * 3 + 2
word 45 = block 22 = 4 * 5 + 2

0	[4, M(32),M(33)]	[2,M(16),M(17)]
1		
2	~~[2,M(20),M(21)]~~ [5,M(44),M(45)]	~~[0,M(4),M(5)]~~ [3,M(28),M(29)]
3		

Block index
(set index)

20(M), 33(M), 21(H), 4(M), 21(H), 17(M), 28(M), 45(M), 33(H)

Question 2:

Compute the total number of bits required to implement a 512KB, 4-way set associative cache with 4-bytes block size (one word/block). Assume that each memory word is 32-bit long and the memory is byte addressable with 32-bits addresses.

Cache size	512KB
Block size	one word
Associativity	4 ways
# of bits for data array	4096 Kbits
# of bits for tag array	1920 Kbits
# of bits for valid bits	128 Kbits
Total # of bits	6144 Kbits

Cache Size: 512KB = 2^{19} bytes
Block Size = 2^2 bytes
# of blocks: $2^{19} / 2^2 = 2^{17}$
# of sets (4 ways) = $2^{17} / 4 = 2^{15}$
# of tag bits (32-2-15) = 15 bits
# of bits for data array = 512*8 = 4096 Kbits
# of bits for tag array = $2^{17} * 15$ = 1920 Kbits
# of bits for valid bits = $2^{17} * 1$ = 128 Kbits
Total # of bits = 6144 Kbits

Question 3: 5

Compute the total number of bits required to implement a 512KB, 2-way set associative cache with 32-bytes block size (8 words/block). Assume that each memory word is 32-bit long and the memory is byte addressable with 32-bits addresses.

Cache size	512KB
Block size	8 words
Associativity	2 ways
# of bits for data array	4096 Kbits
# of bits for tag array	224 Kbits
# of bits for valid bits	16 Kbits
Total # of bits	4336 Kbits

Cache Size: 512KB = 2^{19} bytes
Block Size: 8 words = 2^5 bytes
# of blocks: $2^{19} / 2^5 = 2^{14}$
# of sets (2 ways) = $2^{14} / 2 = 2^{13}$
# of tag bits (32-5-13) = 14 bits
# of bits for data array = 512*8 = 4096 Kbits
# of bits for tag array = 2^{14} * 14 = 224 Kbits
# of bits for valid bits = 2^{14} * 1 = 16 Kbits
Total # of bits = 4336 Kbits

Question 4: 7

Consider a program in which 20% of the instructions are memory load or store instructions, and assume that the CPI for the 5-stage pipeline is 2.5 when the data and instructions are always found in the cache.

1) How many cycles does it take to access the memory if the CPU operates at 2GHz and the memory access latency is 80 n. sec.

Given a 2GHz CPU, the cycle time is 1/(2* 10^9) sec = 0.5 n sec
It takes 160 cycles to access the memory.

2) Assume that the cache miss penalty is equal to the memory access time computed above, what is the average memory access time if the instruction cache miss rate is 2.5% and the data cache miss rate is 5%?

Effective miss rate = 0.025 + 0.05 * 0.2 = 0.035
AMAT = 1 + 0.035 * 160 = 1 + 5.6 = 6.6

3) Assume that an on-chip L2 cache is added to the system, and that the hit time for the L2 cache is 6 cycles. What would be the effective CPI if 70% of the references to the L2 cache (the misses from L1) are found in L2

CPI = 2.5 + 0.035 * (6 + 0.3 * 160) = **4.39**