## Register Allocation

## First Approach: Do Nothing

There is a way to skip the issue

Allocate every variable to memory:

- Locals in activation records
- Globals in data segment
- Member variables Heap allocated variables

Only bring a value from memory when you need it for a calculation.

Immediately store the result back to its memory location.

## Register Allocation

When we generated IR, we held temporary results in virtual registers that we "allocated" from a presumably infinite register file.

When we do code generation, we must face the reality of having a limited set of registers, including those that may have architecture-defined purposes (stack pointer, frame pointer, etc.).

Thus we have a mapping problem: How do we map the elements from the virtual register set into the real architectural registers?

## Naïve Approach Drawbacks

This approach is much too naïve for practical use

Memory accesses are expensive, regardless of the cache structure.
We may have dozens of temporaries whose values are calculated once, used once, and then are never necessary again. This results in huge allocations.

However, this is easy to generate code for and to get right (our \#1 priority in code generation).

Often this is what you will get from a compiler like gcc with no optimizations on (the default).

## Liveness Analysis

```
    x := 0
LOOP: a := x * 2
    x := x + 1
    c := c +
    if a < 100 goto LOOP
    return c;
```



We may note that the idea of saving elements back to memory is unnecessary if we immediately use them again.

Can we identify when a value is useful versus when it does not need to be stored in a register?

Liveness Analysis can tell us the useful range of a value
A value is live if its current value will be useful again at a point in the future.

## Liveness Analysis



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## Control Flow

We have visited the problem of control flow and constructed a control flow graph (CFG) to determine the basic blocks' relation to each other.

Some definitions we will prefer to use:
A CFG node represents a basic block, and by our definition, a basic block has a single entry point and a single exit point.

For each incoming edge to the start of a basic block, we have a control-flow predecessor.

For each outgoing edge from the end of a basic block, we have a control-flow successor.
Defs and
A definition (def) of a variable or temporary occurs when the symbol appears as
the left hand side of an assignment.
A use of a variable is an occurrence of the symbol on the left hand side of an
expression.
We can use these concepts then to describe the set of variable defs and uses that
a node in the CFG defines.
Liveness can then be defined by saying:
A variable is live on a control-flow edge if there is a directed path from that edge to
a use of that variable that does not go through a def.

## Liveness Calculation

Liveness information of each node $n$ of our CFG can be calculated as follows:

- If a node contains a use of a variable, the variable is live on the entry to the block (use[ $n$ ] implies live-in[ $n$ ])
- If a variable is live-in at node $n$, then it is live-out in all of the CFG predecessors of $n$
- If a variable is live-out at node $n$, and not in $\operatorname{def}[n]$, then the variable is also live-in at $n$

In equation form:

$$
\begin{gathered}
\operatorname{in}[n]=\text { use }[n] \cup(\text { out }[n]-\operatorname{def}[n]) \\
\text { out }[n]=\bigcup_{s \in \operatorname{succ}[n]} \text { in }[s]
\end{gathered}
$$

## Liveness Calculation Algorithm

```
for each n
    in[n] }~{
    out[n] - {}
end for
repeat
    for each n //(in reverse DFS order)
        in'[n] \leftarrow in[n]
        out'[n] \leftarrowout[n]
        in[n] \leftarrowuse[n] U (out[n] - def [n])
        out[n] \leftarrow \ \ w succ[n] in[s]
    end for
until in'[n] = in [n] and out[n] = out'[n] for all n
```


## Liveness Analysis



## Liveness Analysis



## Liveness Analysis



## Liveness Analysis




## Liveness Analysis




## Liveness Analysis

| Block 1: |  |  |  |  | Block |  | Def | 1: $x:=0$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  | 6 | c |  | $\square$ |
| $\begin{aligned} & \text { in' }[1]=\operatorname{in}[1]=\{ \} \\ & \text { out' }[1]=\operatorname{out}[1]=\{x\} \\ & \text { in }[1]=\text { use }[1] \cup \text { (out }[1]-\operatorname{def}[1]) \\ & \text { in }[1]=\{ \} \cup(\{x\}-\{x\}) \\ & \text { out }[1]=\operatorname{in}[2]=\{x\} \end{aligned}$ |  |  |  |  |  |  |  | 2: 2 |
|  |  |  |  |  | 4 | c, a | c | 3: $\mathrm{x}:=\mathrm{=x+1}$ |
|  |  |  |  |  | 3 | $\times$ | x | 4: $\mathrm{c}:=\mathrm{c}+\mathrm{a}$ |
|  |  |  |  |  | 2 | x | a | 5: ${ }^{\text {if a }}$ a 100 goto LOOP |
| \| In |  | Out | In | Out | 6: return c; |  |  |  |
| 6 | c |  | c |  |  |  |  |  |
| 5 | a | c | a, c | c, $x$ |  |  |  |  |
| 4 | c, a | a | a, c | a, c |  |  |  |  |
| 3 | x | c, a | a, c, $x$ | a, c |  |  |  |  |
| 2 | x | x | x | a, c, x |  |  |  |  |
| 1 |  | x | x |  |  |  |  |  |



## Liveness Analysis




## Liveness Analysis



## Liveness Analysis



## Liveness Analysis



## Notes on Liveness

The liveness algorithm we have presented will converge regardless of the order that the blocks are visited in, however since out depends on the control flow successors, working in the reverse flow order will generally converge faster.

The algorithm we have presented is conservative: it may overestimate the liveness.

To do this perfectly, we'd have to solve the halting problem.
Since we cannot, we have two choices:

1. Potentially underestimate and have our wrong solution influence our decisions and ultimately produce wrong code
2. Overestimate and sometimes produce code that is not as good as if we had perfect knowledge

## Notes on Liveness (2)

We are much more likely to apply this algorithm at the basic block level rather than the statement level. This also reduces the number of nodes in the graph, something that affects the performance of the algorithm.

The performance of the algorithm depends upon the number of variables, the number of blocks, and how much work the algorithm does each step. In the worst case, the algorithm is $\mathrm{O}\left(\mathrm{n}^{4}\right)$ but in practice, using the reverse CFG order, it is usually $\mathrm{O}\left(\mathrm{n}^{2}\right)$ or less.


## Move (Copy) Instructions

If we have a statement of the form:
$t_{2}:=t_{1}$
And subsequent uses of both $t_{1}$ and $t_{2}$ later in the program, their live ranges overlap and an edge ( $\mathrm{t}_{1}, \mathrm{t}_{2}$ ) would be added to the interference graph.

However, since it is the same value in each, we do not need to keep them in separate registers.

## Building the Interference Graph

Considering this, there are two rules for when to add an edge to the interference graph:

1. A non-move definition of a variable a with live-out variables $b_{1}, \ldots, b_{n}$

- Add edges $\left(a, b_{1}\right)$... $\left(a, b_{n}\right)$

2. A move $a:=c$ with live-out variables $b_{1}, \ldots, b_{n}$

- Add edges $\left(a, b_{1}\right) \ldots\left(a, b_{n}\right)$ for all $b_{i} \neq c$

