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LEI JIN

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Interests

My general interests are in computer architecture and computer system design. Currently, I am working on architectural and OS-based techniques to improve the performance of memory hierarchy.

Education

- **University of Pittsburgh, Pittsburgh, PA** **2004 - Present**
Ph.D student in Computer Science.
GPA: 3.80 / 4.00
- **Zhejiang University, Zhejiang, China** **2000 - 2004**
B.S. in Computer Science, also in Chu Kezhen Honors College, Zhejiang University.
Rank in top 3 in the class and top %3 in the department.
GPA 3.74 / 4.00

Experience

- **Internship at Intel** **2008 Summer**
Microprocessor Technology Laboratory (MTL), Corporate Technology Group (CTG), Intel
- **Graduate Teaching/Research Assistant** **September 2004 - Present**
Department of Computer Science, University of Pittsburgh

Projects

- **Fast Simulation of Multithreaded Applications with Statistical Sampling** **2008 Summer**
I studied and evaluated several sampling techniques to improve the simulation speed of multithreaded applications. In addition to that, dynamic instrumentation technique was used to speedup the functional simulation mode. 10 to 50 times overall speedup was achieved.
- **OS-Based L2 Cache Management** **2006 Spring - Present**
We extend the OS memory management mechanism to flexibly map memory data to distributed L2 caches in multicore processors. I have built a cycle-accurate full-system simulator to perform experiments. Currently, I am exploring the design space of "optimal" page allocation policies to achieve

high performance and low power consumption, as well as necessary architectural support to efficiently implement the OS policies.

- **Digital Photo Frame Development** **2008 Spring**
During this course project, a digital photo frame was developed based on an Altera FPGA board. Visual control was done by software while VGA output was constructed by Verilog.
- **Multiprocessor Memory System Simulator** **2007 Summer**
I developed an execution-driven cycle-accurate multiprocessor memory system simulator based on Simics. This customized simulator models MESI directory coherence protocol implemented in the SGI Origin 2000 server.
- **FIST** **2006 Spring**
I contributed to FIST (a Flexible Instrumentation System for dynamic Translation), built on top of Strata. FIST provides a simple, yet powerful interface to users with different levels of knowledge of the system. It enables the users to construct dynamic instrumentation quickly and efficiently.
- **Macro Data Load** **2004 - 2005**
I designed and studied the macro data load mechanism, which is an efficient mechanism to uncover additional opportunities for load-to-load forwarding by utilizing the spatial locality that exists in cache port wide macro data.
- **Portable Web Browser System** **2004 Spring**
As a bachelor thesis project, we designed and implemented a prototype of portable web browser system. Based on ARM7 processor, VGA display and keyboard input were integrated. Corresponding drivers were developed for uCLinux. A lightweight web browser based on MiniGUI was built from scratch.

Awards

- **Andrew Mellon Predoctoral Fellowship** **September 2007 - June 2008**
University of Pittsburgh

Publications

- Lei Jin and Sangyeun Cho, "**Taming Single-Thread Program Performance on Many Distributed On-Chip L2 Caches**," Proceedings of the International Conference on Parallel Processing (ICPP), Portland, OR, September 2008. To appear.
- Sangyeun Cho, Socrates F. Demetriades, Shayne V. Evans, Lei Jin, Hyunjin Lee, Kiyeon Lee, and Michael Moeng, "**TPTS: A Novel Framework for Very Fast Manycore Processor Simulation**," Proceedings of the International Conference on Parallel Processing (ICPP), Portland, OR, September 2008. To appear.
- Sangyeun Cho, Lei Jin, and Kiyeon Lee, "**Achieving Predictable Performance with On-Chip Shared L2 Caches for Manycore-Based Real-Time Systems**," Proceedings of the IEEE Int'l Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA), pp. 3 11, Daegu, Korea, August 2007. **Invited paper.**

- Lei Jin and Sangyeun Cho, "**Better than the Two: Exceeding Private and Shared Caches via Two-Dimensional Page Coloring**," Proceedings of the Workshop on Chip Multiprocessor Memory Systems and Interconnects (CMP-MSI), during the IEEE Int'l Symposium on High-Performance Computer Architectures (HPCA), Phoenix, Arizona, February 2007.
- Sangyeun Cho and Lei Jin, "**Managing Distributed, Shared L2 Caches through OS-Level Page Allocation**," Proceedings of the IEEE/ACM Int'l Symposium on Microarchitecture (MICRO), Orlando, Florida, December 2006.
Nominated for the best paper award.
- Lei Jin and Sangyeun Cho, "**Reducing Cache Traffic and Energy with Macro Data Load**," Proceedings of the ACM Int'l Symposium on Low Power Electronics and Design (ISLPED), Tegernsee, Germany, October 2006.
- Lei Jin, Hyunjin Lee, and Sangyeun Cho, "**Flexible Page-Level Data Mapping to Cache Slices in Multicore Processors**," Proceedings of the ACM Workshop on Memory Systems Performance and Correctness (MSPC), San Jose, California, October 2006.
- Lei Jin and Sangyeun Cho, "**A Characterization Study on Memory Value Reuse**," Proceedings of the Workshop on Memory Performance Issues (WMPI), Austin, Texas, February 2006.

References

Available upon request.