

SANGYEUN CHO

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Education

Ph.D. in Computer Science, University of Minnesota, December 2002
Thesis Title: A High-Bandwidth Memory Pipeline for Wide-Issue Processors
Thesis Advisors: Pen-Chung Yew and Gyungho Lee

M.S. in Computer Science, University of Minnesota, June 1996

B.S. in Computer Engineering, Seoul National University, Seoul, Korea, *cum laude*, 1994

Appointments

Assistant Professor, September 2004 ~ Present
Department of Computer Science, University of Pittsburgh

Senior Engineer, January 1999 ~ July 2004
Samsung Semiconductor, Giheung, Korea

Intern Software Engineer, June 1998 ~ September 1998
MRL, Intel Corp., Santa Clara, CA

Graduate Teaching/Research Assistant, January 1995 ~ December 1998
Department of Computer Science and Engineering, University of Minnesota

Honors and Awards

- Pitt Computer Science Department Teaching Award (undergraduate core course, 2008/09), 2009.
- Pitt Computer Science Department Teaching Award (undergraduate upper-level course, year 2008/09), 2009.
- Pitt Computer Science Department Teaching Award (graduate course, year 2007/08), 2008.
- A. Richard Newton Graduate Scholarship, the 45th Design Automation Conference (DAC), 2008. This scholarship (\$24,000) is awarded to a faculty PI to support graduate students.
- Research Excellence Award for the work "CalmRISC™-32: A 32-bit Low-Power MCU Core," Samsung Semiconductor, 2001.
- Doctoral Fellowship, Korea Foundation for Advanced Studies (KFAS), 1997, 1998.

Research, Scholarly, and Creative Activities

Refereed Journal Articles

- [J.1] Hyunjin Lee, Lei Jin, Kiyeon Lee, Socrates Demetriades, Michael Moeng, and Sangyeun Cho. "Two-Phase Trace-Driven Simulation (TPTS): A fast multicore processor architecture simulation approach," *Software: Practice and Experience (SPE)*, 27 pages (manuscript), to appear in 2010.
- [J.2] Hyunjin Lee, Sangyeun Cho, and Bruce Childers. "PERFECTION: A Fault-Tolerant Directory Memory Architecture," *IEEE Transactions on Computers (TC)*, 14 pages, to appear in 2010.
- [J.3] Sangyeun Cho and Rami Melhem. "On the Interplay of Parallelization, Program Performance and Energy Consumption," *IEEE Transactions on Parallel and Distributed Systems (TPDS)*, 12 pages, to appear in 2010.
- [J.4] Sangyeun Cho and Lory Al Moakar. "Augmented FIFO Cache Replacement Policies for Low-Power Embedded Processors," *Journal of Circuits, Systems, and Computers (JCSC)*, 18(6):1081~1092, October 2009.
- [J.5] Choongyeun Cho, Daeik Kim, Jonghae Kim, Jean-Olivier Plouchart, Daihyun Lim, Sangyeun Cho, and Robert Trzcinski. "Decomposition and Analysis of Process Variability Using Constrained Principal Component Analysis," *IEEE Transactions on Semiconductor Manufacturing (TSM)*, 21(1):55~62, February 2008.
- [J.6] Sangyeun Cho and Rami Melhem. "Corollaries to Amdahl's Law for Energy," *IEEE Computer Architecture Letters (CAL)*, 7(1):25~28, January 2008. Published on-line in December 2007.
- [J.7] Sangyeun Cho, Pen-Chung Yew, and Gyungho Lee. "A High-Bandwidth Memory Pipeline for Wide Issue Processors," *IEEE Transactions on Computers (TC)*, 50(7):709~723, July 2001.
- [J.8] Sangyeun Cho, Jinseok Kong, and Gyungho Lee. "Coherence and Replacement Protocol of DICE – A Bus-Based COMA Multiprocessor," *Journal of Parallel and Distributed Computing (JPDC)*, 57(1):14~32, April 1999.
- [J.9] Gyungho Lee, Bland W. Quattlebaum, Sangyeun Cho, and Larry L. Kinney. "Design of a Bus-Based Shared-Memory Multiprocessor DICE," *Microprocessors and Microsystems (MM)*, 22(7):403~411, March 1999.
- [J.10] Sangyeun Cho, Jinseok Kong, and Gyungho Lee. "On Timing Constraints of Snooping in a Bus-Based COMA Multiprocessor," *Microprocessors and Microsystems (MM)*, 21(5):313~318, February 1998.

Professional Magazine Articles

- [M.1] Sangyeun Cho, Michael Moeng, and Rami Melhem. "Energy Corollaries to Amdahl's Law," *Microprocessor Report (MPR)*, 10/6/2008 issue, In-Stat, 2008. This publication is an invited, expanded version of [J.6]. *MPR is a premier subscription-only magazine for microprocessor industry executives and professionals.* <http://www.mdronline.com>.
- [M.2] Sangyeun Cho, Tao Li, and Onur Mutlu. "Interaction of Many-core Computer Architecture and Operating Systems," *IEEE Micro*, 28(3):2~5, May/June 2008. This is a Guest Editors' Introduction Article. *IEEE Micro, a bimonthly publication of the IEEE Computer Society, reaches an international audience of microcomputer and microprocessor designers, system integrators, and users.* <http://www.computer.org/portal/web/micro/home>.

Journal Articles in Submission

- [JS.1] Hyunjin Lee, Sangyeun Cho, and Bruce Childers. "DEFCAM: A Design and Evaluation Framework for Defect-Tolerant Cache Memories," a major revision submitted to *ACM Transactions on Architecture and Code Optimization (TACO)*.
- [JS.2] Lei Jin and Sangyeun Cho. "Macro Data Load: An Efficient Mechanism for Enhancing Loaded Value Reuse," a major revision submitted to *IEEE Transactions on Computers (TC)*.

Refereed Conference Publications (acceptance rate shown if known)

- [C.1] Hyunjin Lee, Sangyeun Cho, and Bruce R. Childers. "StimulusCache: Boosting Performance of Chip Multiprocessors with Excess Cache," *Proceedings of the IEEE International Symposium on High-Performance Computer Architecture (HPCA)*, Bangalore, India, January 2010.
- [C.2] Sangyeun Cho and Hyunjin Lee. "Flip-N-Write: A Simple Deterministic Technique to Improve PRAM Write Performance, Energy and Endurance," *Proceedings of the IEEE/ACM International Symposium on Microarchitecture (MICRO)*, New York City, NY, December 2009.
- [C.3] Michel Hanna, Socrates Demetriades, Sangyeun Cho, and Rami Melhem, "Progressive Hashing for Packet Processing Using Set-Associative Memory," *Proceedings of the ACM/IEEE Symposium on Architectures for Networking and Communications Systems (ANCS)*, Princeton, NJ, October 2009. Acceptance rate ~23% (17/73).
- [C.4] Lei Jin and Sangyeun Cho. "SOS: A Software-Oriented Distributed Shared Cache Management Approach for Chip Multiprocessors," *Proceedings of the 18th International Conference on Parallel Architectures and Compilation Techniques (PACT)*, Raleigh, NC, September 2009. Acceptance rate ~19% (35/188).
- [C.5] Mohammad H. Hammoud, Sangyeun Cho, and Rami Melhem. "Dynamic Cache Clustering for Chip Multiprocessors," *Proceedings of the ACM International Conference on Supercomputing (ICS)*, pp. 56~67, IBM T. J. Watson Research Center, NY, June 2009. Acceptance rate ~25% (47/191).
- [C.6] Taecheol Oh, Hyunjin Lee, Kiyeon Lee, and Sangyeun Cho, "An Analytical Model to Study Optimal Area Breakdown between Cores and Caches in a Chip Multiprocessor," *Proceedings of the IEEE Computer Society Symposium on VLSI (ISVLSI)*, pp. 181~186, Tampa, FL, May 2009.
- [C.7] Michel Hanna, Socrates Demetriades, Sangyeun Cho, and Rami Melhem, "CHAP: Enabling Efficient Hardware-based Multiple Hash Scheme for IP Lookup," *Proceedings of the IFIP International Conference on Networking (Networking)*, pp. 756~769, Aachen, Germany, May 2009. Acceptance rate ~20% (46/229).
- [C.8] Kiyeon Lee, Shayne Evans, and Sangyeun Cho, "Accurately Approximating Superscalar Processor Performance from Traces," *Proceedings of the IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, pp. 238~248, Boston, MA, April 2009. Acceptance rate ~28% (24/86).
- [C.9] Mohammad H. Hammoud, Sangyeun Cho, and Rami Melhem. "ACM: An Efficient Approach for Managing Shared Caches in Chip Multiprocessors," *Proceedings of the 4th International Conference on High Performance and Embedded Architectures and Compilers (HiPEAC)*, pp. 355~372, Paphos, Cyprus, January 2009. Acceptance rate ~28% (27/97).
- [C.10] Choongyeun Cho, Daeik Kim, Jonghae Kim, Daihyun Lim, and Sangyeun Cho. "Early Prediction of Product Performance and Yield via Technology Benchmark," *Proceedings of the IEEE Custom Integrated Circuits Conference (CICC)*, pp. 205~208, San Francisco, CA, September 2008.
- [C.11] Lei Jin and Sangyeun Cho. "Taming Single-Thread Program Performance on Many Distributed On-Chip L2 Caches," *Proceedings of the International Conference on Parallel Processing (ICPP)*, pp. 487~494, Portland, OR, September 2008. Acceptance rate ~31% (81/263).
- [C.12] Sangyeun Cho, Socrates Demetriades, Shayne Evans, Lei Jin, Hyunjin Lee, Kiyeon Lee, and Michael Moeng. "TPTS: A Novel Framework for Very Fast Manycore Processor Simulation," *Proceedings of the International Conference on Parallel Processing (ICPP)*, pp. 446~453, Portland, OR, September 2008. Acceptance rate ~31% (81/263).
- [C.13] Socrates Demetriades, Michel Hanna, Sangyeun Cho, and Rami Melhem. "An Efficient Hardware-based Multi-hash Scheme for High Speed IP Lookup," *Proceedings of the Annual IEEE Symposium*

on *High-Performance Interconnects (HOTI)*, pp. 103~110, Stanford, CA, August 2008. Acceptance rate ~30% (14/47).

- [C.14] Jongbae Kim, Sangyeun Cho, and Seung-Jae Kim. "Preliminary Studies to Develop a Ubiquitous Computing and Health-monitoring System for Wheelchair Users," *Proceedings of the ACM International Conference on Body Area Networks (BodyNets)*, Tempe, AZ, March 2008.
- [C.15] Hyunjin Lee, Sangyeun Cho, and Bruce Childers. "Exploring the Interplay of Yield, Area, and Performance in Processor Caches," *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, pp. 216~223, Lake Tahoe, CA, October 2007.
- [C.16] Sangyeun Cho, Lei Jin, and Kiyeon Lee. "Achieving Predictable Performance with On-Chip Shared L2 Caches for Manycore-Based Real-Time Systems," *Proceedings of the IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA)*, pp. 3~11, Daegu, Korea, August 2007. **Invited paper.**
- [C.17] Hyunjin Lee, Sangyeun Cho, and Bruce R. Childers. "Performance of Graceful Degradation for Cache Faults," *Proceedings of the IEEE Computer Society Symposium on VLSI (ISVLSI)*, pp. 409~415, Porto Alegre, Brazil, May 2007.
- [C.18] Sangyeun Cho, Joel R. Martin, Ruibin Xu, Mohammad H. Hammoud, and Rami Melhem, "CA-RAM: A High-Performance Memory Substrate for Search-Intensive Applications," *Proceedings of the IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, pp. 230~241, San Jose, CA, April 2007. Acceptance rate ~30% (24/79).
- [C.19] Choongyeun Cho, Daeik Kim, Jonghae Kim, Jean-Olivier Plouchart, Daihyun Lim, Sangyeun Cho, and Robert Trzcinski. "A Data-Driven Statistical Approach to Analyzing Process Variation in 65nm SOI Technology," *Proceedings of the International Symposium on Quality Electronic Design (ISQED)*, San Jose, CA, March 2007. Acceptance rate ~32% (93/292).
- [C.20] Sangyeun Cho. "I-Cache Multi-Banking and Vertical Interleaving," *Proceedings of the ACM Great Lakes Symposium on VLSI (GLSVLSI)*, Stresa-Lago Maggiore, Italy, March 2007. Acceptance rate ~21% (68/324).
- [C.21] Sangyeun Cho and Lei Jin. "Managing Distributed, Shared L2 Caches through OS-Level Page Allocation," *Proceedings of the IEEE/ACM International Symposium on Microarchitecture (MICRO)*, pp. 455~465, Orlando, FL, December 2006. Acceptance rate ~24% (42/174). **Nominated for the best paper award (11/174=~6%).**
- [C.22] Lei Jin and Sangyeun Cho. "Reducing Cache Traffic and Energy with Macro Data Load," *Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED)*, pp. 147~150, Tegernsee, Germany, October 2006. Acceptance rate ~35% (75/214).
- [C.23] Sangyeun Cho, Seung-Jae Chung, Sang-Hyun Park, Sangwoo Kim, Sungjin Jung, Wooyoung Jung, Sanghoon Moon, and Yong-Chun Kim. "CPAD4: A Highly Integrated Low Power Digital Audio Chip," *Proceedings of the IEEE Symposium on Low-Power and High-Speed Chips (Cool Chips)*, Tokyo, Japan, April 2002.
- [C.24] Sangyeun Cho, Wooyoung Jung, Yong-Chun Kim, and Seh-Woong Jeong. "A Low-Power Cache Design for CalmRISC™-Based Systems," *Proceedings of the International Conference on Computer Design (ICCD)*, pp. 394~399, Austin, TX, September 2001.
- [C.25] Chang-Ho Lee, Hoon-Mo Yang, Seung-Ho Kwak, Moon-Key Lee, Sanghyun Park, Sangyeun Cho, Sangwoo Kim, Yongchun Kim, Seh-Woong Jeong, Bong-Young Chung, and Hyung-Lae Roh. "Efficient Random Vector Verification Method for an Embedded 32-bit MCU Core," *Proceedings of the 2nd IEEE Asia-Pacific Conference on ASICs (AP-ASIC)*, pp. 291~294, Jeju, Korea, August 2000.

- [C.26] Sangyeun Cho, Sanghyun Park, Sangwoo Kim, Yongchun Kim, Seh-Woong Jeong, Bong-Young Chung, Hyung-Lae Roh, Chang-Ho Lee, Hoon-Mo Yang, Seung-Ho Kwak, and Moon-Key Lee. "CalmRISC™-32: A 32-Bit Low Power MCU Core," *Proceedings of the 2nd IEEE Asia-Pacific Conference on ASICs (AP-ASIC)*, pp. 285~289, Jeju, Korea, August 2000.
- [C.27] Sangyeun Cho, Pen-Chung Yew, and Gyungho Lee. "Access Region Locality for High-Bandwidth Processor Memory System Design," *Proceedings of the 32nd IEEE/ACM International Symposium on Microarchitecture (MICRO)*, pp. 136~146, Haifa, Israel, November 1999. Acceptance rate ~21% (27/131).
- [C.28] Sangyeun Cho, Pen-Chung Yew, and Gyungho Lee. "Decoupling Local Variable Accesses in a Wide-Issue Superscalar Processor," *Proceedings of the 26th ACM/IEEE International Symposium on Computer Architecture (ISCA)*, pp. 100~110, Atlanta, GA, May 1999. Acceptance rate ~19% (26/135).
- [C.29] Sangyeun Cho, Jenn-Yuan Tsai, Yonghong Song, Bixia Zheng, Steve J. Schwinn, Xin Wang, Qing Zhao, Zhiyuan Li, David Lilja, and Pen-Chung Yew. "High-Level Information – An Approach for Integrating Front-End and Back-End Compilers," *Proceedings of the International Conference on Parallel Processing (ICPP)*, pp. 346~355, Minneapolis, MN, August 1998. Acceptance rate ~34%.
- [C.30] Gyungho Lee, Bland Quattlebaum, Sangyeun Cho, and Larry Kinney. "Global Bus Design of a Bus-Based COMA Multiprocessor DICE," *Proceedings of the 8th IEEE International Conference on Computer Design (ICCD)*, pp. 231~240, Austin, TX, October 1996.
- [C.31] Sangyeun Cho and Gyungho Lee. "Reducing Coherence Overhead in Shared-Bus Multiprocessors," *Proceedings of EURO-PAR*, pp. 492~497, Lyon, France, August 1996.

Refereed/Invited Workshop Publications

- [W.1] Lei Jin and Sangyeun Cho. "Better than the Two: Exceeding Private and Shared Caches via Two-Dimensional Page Coloring," *Proceedings of the Workshop on Chip Multiprocessor Memory Systems and Interconnects (CMP-MSI)*, during the *IEEE International Symposium on High-Performance Computer Architecture (HPCA)*, Phoenix, AZ, February 2007.
- [W.2] Sangyeun Cho and Rami Melhem. "A Scalable and Reconfigurable Search Memory Substrate for High Throughput Packet Processing," *Proceedings of the IEEE 21st Computer Communications Workshop (CCW)*, Pittsburgh, PA, February 2007. **Invited presentation.**
- [W.3] Lei Jin, Hyunjin Lee, and Sangyeun Cho. "A Flexible Data to L2 Cache Mapping Approach for Future Multicore Processors," *Proceedings of the ACM Workshop on Memory Systems Performance and Correctness (MSPC)*, during the *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, pp. 92~101, San Jose, CA, October 2006.
- [W.4] Lei Jin and Sangyeun Cho. "A Characterization Study on Memory Value Reuse," *Proceedings of the Workshop on Memory Performance Issues (WMPI)* during the *IEEE International Symposium on High-Performance Computer Architecture (HPCA)*, Austin, TX, February 2006.

Patents

- [P.1] Sangyeun Cho and Wooyoung Jung. "Cache memory system having a flexible buffer memory portion and methods of operating the same," US patent pending; disclosed in January 2005.
- [P.2] Sangyeun Cho. "System and controller with reduced bus utilization time," US patent 7,543,114, June 2009.

- [P.3] Sangyeun Cho. "Memory controller having a read-modify-write function," US patent 7,299,323, November 2007.
- [P.4] Sangyeun Cho and Yongchun Kim. "Apparatus and method for testing on-chip ROM," US patent 7,134,063, November 2006.
- [P.5] Sangyeun Cho. "Microprocessor having a low-power cache memory," US patent 6,934,811, August 2005.
- [P.6] Sangyeun Cho and Gyungho Lee. "Self-invalidation method for reducing coherence overheads in a bus-based shared-memory multiprocessor apparatus," US patent 5,835,950, November 1998.

Grants and Contracts*

- [G.1] EAGER: CA-RAM: Enabling Fast and Versatile Packet Processing for Future Large-Scale Networks
Sangyeun Cho (PI)
National Science Foundation (NSF)
Award amount: \$150,000
Award period: September 2009 ~ August 2011
- [G.2] TPTS: A Very Fast Simulation Framework for Next-Generation Many-Core Processor Architecture Research
Sangyeun Cho (PI)
University of Pittsburgh Central Research Development Fund
Award amount: \$15,750
Award period: July 2009 ~ June 2011
- [G.3] Hardware Abstraction and Modeling Methods for Predicting Multicore Embedded System Performance
Sangyeun Cho (PI)
Samsung Advanced Institute of Technology (SAIT)
Award amount: \$35,000
Award period: March 2009 ~ August 2009
- [G.4] WORKSHOP: Support for the 15th International Symposium on High-Performance Computer Architecture (HPCA-15)
Sangyeun Cho (PI)
National Science Foundation (NSF)
Award amount: \$10,000
Award period: January 2009 ~ June 2009
- [G.5] Bridging Technology Fragility and Next-Generation Many-Core Processor Architectures and Systems Research (A. Richard Newton Graduate Scholarship)
Sangyeun Cho (PI)
ACM Design Automation Conference (DAC)
Award amount: \$24,000
Award period: May 2008 ~ April 2009
- [G.6] Test and Continuous Adaptive Repair of Multicore Memory Hierarchies in Nanoscale Technology
Bruce Childers (PI), Sangyeun Cho (co-PI)
National Science Foundation (NSF)
Award amount: \$400,000
Award period: July 2007 ~ June 2010
- [G.7] Processor Performance Characterization in the Presence of Transient Errors
Sangyeun Cho (PI)
University of Pittsburgh Central Research Development Fund
Award amount: \$14,400
Award period: July 2005 ~ June 2007

* This section lists grants that have been awarded. There are three pending proposals that have been submitted to NSF, DOE, and NIST as of October 10, 2009.

Teaching

Term	Course	Student Evaluation*
Spring 2009	CS 3410 (G) Advanced Topics in Computer Architecture	4.75/5 10/10
Spring 2009	CS/COE 1541(UG) Introduction to Computer Architecture	4.68/5 10/10
Fall 2008	CS/COE 0447 (UG) Computer Organization and Assembly Language	4.33/5 8/10
Spring 2008	CS/COE 0447 (UG) Computer Organization and Assembly Language	4.30/5 8/10
Spring 2008	CS/COE 1541 (UG) Introduction to Computer Architecture	3.78/5 4/10
Fall 2007	CS/COE 2410 (G) Computer Architecture	4.08/5 6/10
Spring 2007	CS 3410 (G) Advanced Topics in Computer Architecture	NA**
Spring 2007	CS/COE 1541 (UG) Introduction to Computer Architecture	3.37/5 2/10
Fall 2006	CS 2410 (G) Computer Architecture	4.38 8/10
Spring 2006	CS/COE 0447 (UG) Computer Organization and Assembly Language	3.75/5 4/10
Fall 2005	CS 2410 (G) Computer Architecture	3.89/5 5/10
Spring 2005	CS 3410 (G) Advanced Topics in Computer Architecture	NA**
Fall 2004	CS/COE 0447 (UG) Computer Organization and Assembly Language	3.61/5 3/10

* The evaluation is conducted by the Office of Measurement and Evaluation of Teaching (OMET). Students rate the overall effectiveness of the instructor on a five point scale. The averaged score is normalized against the "Fall 1997 results of 157 undergraduate classes taught by tenured and tenure-stream faculty within the Arts & Sciences who were selected to participate in the norming of the revised instrument." This table reports both the average scores and the deciles, which "divide the distribution of class means for each item in the random sample into ten subgroups of equal frequency."

** Quantitative survey was not performed for these seminar courses because the enrollments were low.

Graduate Student Supervision

Current Students (as of year 2009~2010)

Socrates Demetriades	Ph.D. student, year 4, co-advised with Rami Melhem
Mohammad H. Hammoud	Ph.D. student, year 5, co-advised with Rami Melhem (primary advisor)
Michel Hanna	Ph.D. student, year 5, co-advised with Rami Melhem (primary advisor)
Lei Jin	Ph.D. candidate since 2009, year 6
Hyunjin Lee	Ph.D. student, year 5, co-advised with Bruce Childers
Kiyeon Lee	Ph.D. student, year 4
Michael Moeng	Ph.D. student, year 3, co-advised with Rami Melhem
Taecheol Oh	Ph.D. student, year 4
Musfiq Rahman	Ph.D. student, year 3, co-advised with Bruce Childers (primary advisor)

Graduated Students

Shayne Evans	M.S. in 2008. First appointment with Lime Brokerage LLC.
Marius Giurgi	M.S. in 2006. First appointment with Blue Belt Technologies.

Ph.D. Dissertation Committee

Ali Alanjawi	Ph.D. in 2009, advisor: Bob Daley.
José A. Baiocchi	Ph.D. candidate since 2009, advisor: Bruce Childers.
Naveen Kumar	Ph.D. in 2008, advisors: Bruce Childers and Mary Lou Soffa.
Shuyi Shao	Ph.D. candidate since 2007, advisors: Rami Melhem and Alex Jones.

Synergistic Professional Activities

Editorial Board

- Guest co-editor: IEEE Micro Special Issue on Interaction of Computer Architecture and Operating Systems in the Many-core Era, May/June 2008.
- Volume co-editor: Advances in Computer Systems Architecture, Proceedings of the 12th Asia-Pacific Computer Systems Architecture Conference (ACSAC), Lecture Notes in Computer Science 4697, Springer, August 2007.

Organizing Committee

- Publicity co-chair: The 39th Int'l Conference on Parallel Processing (ICPP), 2010.
- Student travel chair: The 15th Int'l Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2010.
- Workshop co-organizer: Workshop on the Interaction between Operating System and Computer Architecture (WIOSCA), 2009.
- Student affairs chair: The 15th Int'l Symposium on High-Performance Computer Architecture (HPCA), 2009.
- Workshop co-organizer: Workshop on the Interaction between Operating System and Computer Architecture (WIOSCA), 2008.
- Program co-chair: The 12th Asia-Pacific Computer Systems Architecture Conference (ACSAC), 2007.
- Workshop co-organizer: Workshop on the Interaction between Operating System and Computer Architecture (WIOSCA), 2007.
- Workshop co-organizer and general chair: The 11th Workshop on Interaction between Compilers and Computer Architectures (INTERACT), 2007.
- Registration Chair. The 12th Int'l Conference on Parallel and Distributed Systems (ICPADS), 2006.
- Workshop co-organizer and program committee chair: The 10th Workshop on Interaction between Compilers and Computer Architectures (INTERACT), 2006.

Technical Program Committee

- The 15th Int'l Conference on Parallel and Distributed Systems (ICPADS), 2009.
- The IEEE Int'l Conference on Networking, Architecture, and Storage (NAS), 2009.
- The 13th Workshop on Interaction between Compilers and Computer Architectures (INTERACT), 2009.
- The Int'l Conference on Parallel Processing (ICPP), 2008.
- The 13th Int'l Conference on Parallel and Distributed Systems (ICPADS), 2007.
- The ACM Symposium on Applied Computing (SAC), SoC Design and Software Support Track, 2007.
- The Int'l Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), 2006.
- The 11th Asia-Pacific Computer Systems Architecture Conference (ACSAC), 2006.
- The IEEE Int'l Symposium on Performance Analysis of Systems and Software (ISPASS), 2006.
- The 10th Asia-Pacific Computer Systems Architecture Conference (ACSAC), 2005.
- The IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2005.
- The 9th Workshop on Interaction between Compilers and Computer Architectures (INTERACT), 2005.
- The 9th Asia-Pacific Computer Systems Architecture Conference (ACSAC), 2004.
- The 8th Workshop on Interaction between Compilers and Computer Architectures (INTERACT), 2004.

Reviewer

- Journals: ACM Transactions on Embedded Computing Systems (TECS), IEEE Transactions on Computers (TC), IEEE Transactions on Parallel and Distributed Systems (TPDS), IEEE Transactions on Very Large-Scale Integration Systems (TVLSI), Journal of Parallel and Distributed Computing (JPDC), The Computer Journal

(COMPJ), Journal of Computer Science and Technology (JCST), Journal of Computer Languages, Systems, and Structures (JCLSS), ETRI Journal, IPSI Transactions on Internet Research

- Conferences: International Symposium on Computer Architecture (ISCA), International Symposium on High-Performance Computer Architecture (HPCA), International Symposium on Microarchitecture (MICRO), International Symposium on High-Performance Interconnects (HOTI), International Conference on Parallel Architectures and Compilation Techniques (PACT), International Conference on Computer Design (ICCD), International Conference on Parallel Processing (ICPP), International Conference on Supercomputing (ICS), International Solid-State Circuits Conference (ISSCC), International Symposium on Low-Power Electronics and Design (ISLPED), Asia-Pacific Computer Systems Architecture Conference (ACSAC)

[Grant proposal panelist/reviewer](#)

- Internal Research Funding competition, University of Cyprus, 2009.
- CRDF (Central Research Development Fund) grant competition, University of Pittsburgh, 2008.

Invited Talks

- "Two Mechanisms for Distributed On-Chip L2 Cache Management in Chip Multiprocessors," presented at the ECE Department, Hanyang University, Seoul, Korea, August 2009.
- "Two Mechanisms for Distributed Shared Cache Management in Chip Multiprocessors," presented at the ECE Department, University of Wisconsin, Madison, WI, May 2009.
- "An OS-based Shared L2 Cache Management Approach for Many-core Processors," presented at Intel Systems Technology Lab (STL), Hillsboro, OR, September 2008.
- "An OS-based Shared L2 Cache Management Approach for Many-core Processors," presented at Institute of Computing Technology (ICT), Chinese Academy of Science (CAS), Beijing, China, June 2008.
- "Revisiting Parallel Programming Practices and Issues," presented at Samsung Advanced Institute of Technology (SAIT), Giheung, Korea, August 2007.
- "Flexibly Managing Distributed L2 Caches in Many-Core Processors," presented at the ECE Department, North Carolina State University, Raleigh, NC, April 2007.
- "Malleable Many-Core Architectures," presented at Microsoft Research, Redmond, WA, March 2007.
- "Managing Distributed Shared L2 Caches through OS-Level Page Allocation," presented at CALCM, Carnegie Mellon University, Pittsburgh, PA, November 2006.
- "Memory Hierarchy Design Issues in Future Multicore Processors, An Architect's Point of View," presented at Samsung Advanced Institute of Technology (SAIT), Giheung, Korea, August 2006.
- "A Flexible L2 Cache Management Approach for Future Multicore Processors," presented at School of EECS, Seoul National University, Seoul, Korea, August 2006.
- "A High-Bandwidth Memory Pipeline for Wide-Issue Processors," presented at School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN, March 2004.
- "Designing an Embedded Processor for Media SOCs," presented at School of Electrical and Computer Engineering, Handong University, Pohang, Korea, April 2003.
- "CalmRISC™-32, A Low-Power MCU Core for Portable Applications," presented at School of Electrical and Computer Engineering, Handong University, Pohang, Korea, March 2001.

Department/University Services

- Organizing Committee, The Pitt CS Day, 2008~2009.
- Organizing Committee, The Pitt CS Day; organized the first Video/Graphic Contest, 2007.
- Leader, Computer Science Graduate Recruiting Task Force, 2006.
- Computer Science Graduate Admissions and Financial Aid Committee (GAFA), 2005~2007.
- Computer Science Undergraduate Recruiting and Advising Committee (UGRAC), 2004~2005.