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CS/COE 0447 Example Problems for Exam 2
Spring 2011

1) Show the steps to multiply the 4-bit numbers 3 and 5 with the "fast shift-add multipler". Use the table below. List the multiplicand (M) and product (P) in binary. In the field "step", write "ADD" when the multiplicand is added. Write "SHIFT" to indicate when the product is shifted. In the iteration "Start" write the initial values for the mutiplicand and product. You may not need all steps (rows) in the table.

Iter.	Multiplicand (M)	Product (P)	Step
Start			
1			
2			
3			
4			
5			
6			
7			

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2) Show the steps to multiply an 6-bit number 17 and 3 with Booth's algorithm. Use the table below. List the multiplicand and product in binary. In the field "step", write "ADD", "SUB", or "NO OP" to indicate which operation is done on each iteration.

Iter.	Multiplicand (M)	Product (P)	Step
Start			
1			
2			
3			
4			
5			
6			
7			

3) Explain how the "fast shift-add multiply" improves over the original "slow shift-add multiply". Be sure to indicate what hardware changes make the "fast version" faster than the "slow version".

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4) Consider restoring division with hardware design #3 (the design with a 32-bit divisor and a 64-bit remainder register that holds the remainder and quotient). Assume the quotient and divisor are 5 bit unsigned numbers. Fill in the table below for 17 / 3. For each step, indicate what shift, subtraction, and addition operations are done in the "Step Notes" column.

Iteration	**Divisor (D)**	**Remainder (R)**	**Notes**
Init			
1			
2			
3			
4			
5			
6			
Done			

5) Suppose we want to do the computation S = A + B. A and B are positive 2's complement 8-bit binary numbers. Give a boolean expression that indicates whether there was an overflow when these numbers are added. To represent a certain bit *i* in *A*, *B* or *S*, use A_i, B_i or S_i. E.g., bit position 3 in *A* is A_3. Assume the bits are numbered 0 to 7 (right to left).

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6) Give the negation in one's complement binary representation (5 bit numbers) for the decimal numbers:

5d Negation (in one's complement binary) _____

10d Negation (in one's complement binary) _____

-15d Negation (in one's complement binary) _____

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7) Give the negation in two's complement binary representation (5 bits) for the decimal numbers:

   11d Negation (in two's complement binary) _____

   15d Negation (in two's complement binary) _____

   -13d Negation (in two's complement binary) _____

8) Give Booth's encoding for the 8-bit numbers:

   -19d Booth's encoding _____

   -

   27d Booth's encoding _____

   62d Booth's encoding _____

9) Give *two reasons* to use Booth's algorithm (encoding) to improve the multiplication hardware.

10) Floating-point numbers represent a "richer" set of values than integer numbers. Nevertheless, processors support integer numbers and programs frequently use them. What primary advantage does integer numbers and operations offer over floating point numbers and operations?

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11) Using 1-bit adders, draw the circuit for a 4-bit ripple-carry addition unit.

12) Using 1-bit adders and 1-bit inverters (i.e., the *not* of a bit), draw a circuit for a 4-bit ripple-carry subtract unit.

13) Consider the sum of products boolean equation: A'BC + ABC + A'B'C. Give the truth table representation for this boolean equation. (A' is NOT A and + is OR)

14) Suppose you want to design a hardware circuit that has two inputs A and B, and one output O. The output O has the value 1 when exactly one input (A/B) is a 1. Give the truth table for this circuit design.

INPUTS		***OUTPUT***
A	***B***	***O***

15) For question 15, what is the boolean equation for the truth table?

16) Here is a truth table. What is the boolean equation for O?

INPUTS			**OUTPUT**
A	**B**	**C**	**O**
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

17) Let's consider a 4-bit adder. If each 1-bit adder takes 2ns to compute an output (1-bit result and carry-out), how long does it take to compute the full 4-bit result?

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18) Consider problem 17 again. This time, let's compute the time for subtraction (A-B). Suppose the 1-bit inverter (used to complement the B input of each 1-bit adder) takes 1ns. How long does it take to compute an answer with this subtraction unit? (*Be careful*: Think about whether the invert operations can be done simultaneously.)

19) Consider the logic function: F = A'BC' + A'BC + AB'C + ABC. Draw a K-map for this function, circle the minimum terms (1s), and give the simplified Boolean equation.

		C	
		0	1
AB	00		
	01		
	11		
	10		

20) Given the K-map below, what is the simplified Boolean equation?

		CD			
		00	**01**	**11**	**10**
AB	**00**	0	0	0	0
	01	0	0	0	0
	11	0	1	1	0
	10	0	1	1	0

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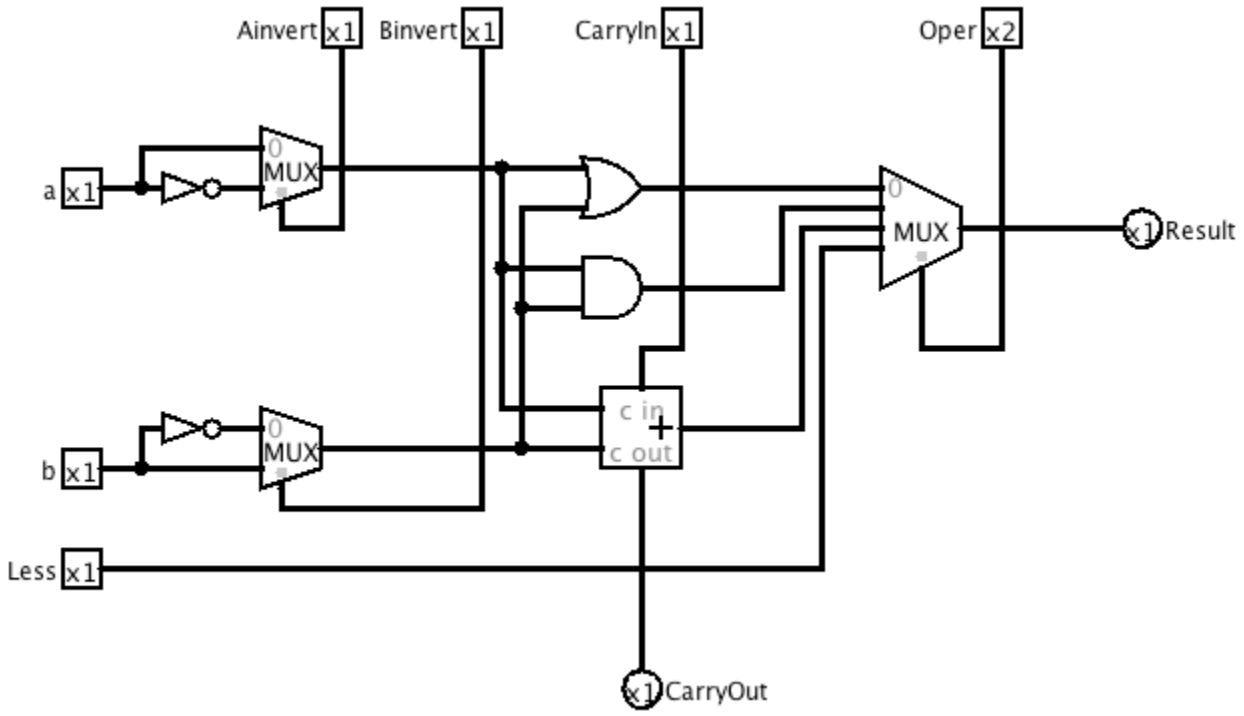
21) Given the K-map below, what is the simplified Boolean equation?

		CD			
		00	**01**	**11**	**10**
AB	**00**	1	1	0	0
	01	0	0	1	1
	11	0	0	1	1
	10	0	0	0	0

22) Consider the ALU below. Note this ALU has some minor wiring differences than the one described in class. Answer the questions below for this ALU.



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To perform addition, how should Ainvert, Binvert, CarryIn and Oper be set (if the input doesn't matter, use an 'X')?

To perform an OR operation, how should Ainvert, Binvert, CarryIn and Oper be set (if the input doesn't matter, use an 'X')?

To perform a NAND operation, how should Ainvert, Binvert, CarryIn and Oper be set (if the input doesn't matter, use an 'X')?

To perform a NOR operation, how should Ainvert, Binvert, CarryIn and Oper be set (if the input doesn't matter, use an 'X')?

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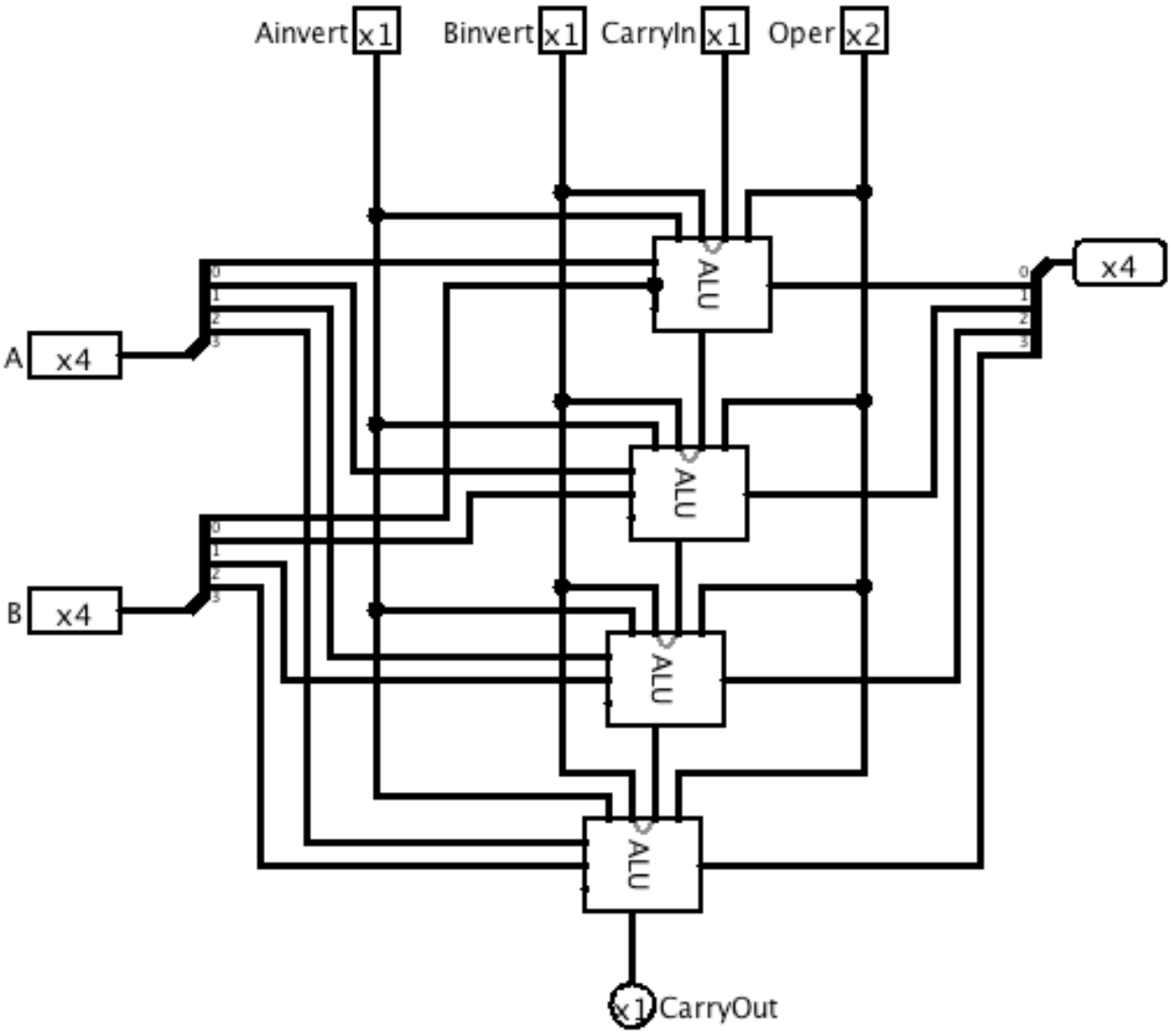

23) Consider the 4-bit ALU (figure above) made with the 1-bit ALU from the previous questions. Suppose, Ainvert=0, Binvert=0, CarryIn=1, A=0100, B=0011, and Oper=10. What is Result?

24) Now, suppose, Ainvert=0, Binvert=0, CarryIn=1, A=0101, B=0011, and Oper=00. What is the result?