

# HYUNJIN A. LEE

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## CONTACT INFORMATION

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## RESEARCH INTERESTS

Low power microprocessor architecture, multicore architecture, memory system, fault-tolerant processor architectures, and high-speed processor architecture simulation methods

## EDUCATION

**University of Pittsburgh**, Pittsburgh, PA, USA  
Ph.D. Computer Science, August 2011  
Advisors: Sangyeun Cho and Bruce R. Childers

**Seoul National University**, Seoul, Korea  
B.S., Electrical Engineering, February 1999

## ACADEMIC EXPERIENCE

**University of Pittsburgh**, Pittsburgh, PA, USA  
*Graduate Student Researcher*

**September 2005 – July 2011**

Duties include current Ph.D. research, graduate level course work and research projects

- Scalable and flexible last level cache substrate for many-core CMPs
- Improving performance of chip multiprocessors with excess cache
- Fault-tolerant on-chip directory memory
- Performance analysis of cache memory with various fault masking schemes
- Development of a unified cache design platform for processor architects to consider yield, performance and cost in an early design stage
- Contribution to the development of a very fast multi-core processor simulator based on the notion of two-phase trace-driven simulation

*Teaching Fellow* (Primary Instructor)

Duties include lectures, office hours, examination and project creation, advising TAs

- CS 0449: Introduction to Systems Software

**Summer 2010**

*Teaching Assistant* (Recitation Leader)

Duties include selected lectures, office hours, examination and quiz creation, developing and leading computer lab exercises.

- CS 0447: Computer Organization and Assembly Language **Spring/Fall 2006, Spring 2007**
- CS 1510: Algorithm Design **Fall 2006**
- CS 1502: Formal Methods in Computer Science **Summer/Fall 2007**

**Seoul National University (SNU)**, Seoul, Korea

*Undergraduate Student Researcher*

**March 1998 – December 1998**

Duty Includes research projects at *System Design Lab, SNU*

- Design of a 32-bit CPU using Synopsis and VHDL
- Research on discrete cosine transform motion estimation technique

## PROFESSIONAL EXPERIENCE

**Intel Labs**, Santa Clara, California  
Research Scientist

September 2011 – present

- Work on Ultra Low Power Processor Architecture

**Microsoft Research**, Redmond, Washington  
Research Intern

August 2010 – October 2010

- Worked on Efficient Distributed Tuple Space project
- Designed system software blocks for Microsoft datacenter

**Samsung Semiconductor**, Giheung, Korea  
Engineer

April 2004 – April 2005

- Worked on DVD-Recorder SOC (system on chip) projects
- Tested and verified Samsung's DVD-Recorder chipsets
- Designed image framing software blocks for DVD-R/DVD-RW/DVD+RW

**PrimeMover Inc.**, Seoul, Korea  
Engineer

October 2002 – March 2004

- Developed DVR (Digital Video Recorder) software based on embedded Linux.
- Designed JPEG image processing block (for still image capture)
- Managed manufacturing process for the mass products

**3R Technologies Inc.**, River Edge, New Jersey/ Seoul, Korea  
Engineer

January 1999 – July 2002

- Designed JPEG image processing block and system managing software
- Developed ATM (Asynchronous Transfer mode) Unit software using VxWorks (WindRiver), MPC860 (Motorola) and Vortex chipset (PMC-Sierra)
- Designed AM (alarm mgmt.), PM (performance monitoring), TM (traffic mgmt.), OAM (operation administration mgmt.), IPC, and STM-1/STS-4 layer management software blocks
- Designed DMT (discrete multitone) chipset control and peripheral blocks using FPGA (Xilinx)

## PUBLICATIONS

### Refereed Journal Articles

- [J.1] **Hyunjin Lee**, Sangyeun Cho, and Bruce R. Childers. "DEFCAM: A Design and Evaluation Framework for Defect-Tolerant Cache Memories," *ACM Transactions on Architecture and Code Optimization (TACO)*, 8(3): Article 17, October 2011
- [J.2] **Hyunjin Lee**, Sangyeun Cho, and Bruce R. Childers. "PERFECTION: A Fault-Tolerant Directory Memory Architecture", *IEEE Transactions on Computer (TC)*, 59(5):638~650, May 2010
- [J.3] **Hyunjin Lee**, Lei Jin, Kiyeon Lee, Socrates Demetriades, Michael Moeng, and Sangyeun Cho. "Two-Phase Trace-driven Simulation (TPTS): A fast multicore processor architecture simulation approach", *Software: Practice and Experience (SPE)*, 40(3):239~258, March 2010

### Refereed Conference Publications

- [C.1] **Hyunjin Lee**, Sangyeun Cho, and Bruce R. Childers. "CloudCache: Expanding and Shrinking Private Caches," *IEEE International Symposium on High-Performance Computer Architecture (HPCA)*, San Antonio, Texas, February 2011. Acceptance rate ~ 18.5% (42/227)
- [C.2] **Hyunjin Lee**, Sangyeun Cho, and Bruce R. Childers. "StimulusCache: Boosting Performance of Chip Multiprocessors with Excess Cache" *IEEE International Symposium on High-Performance Computer Architecture (HPCA)*, Bangalore, India, January 2010. Acceptance rate ~18.3% (32/175).
- [C.3] Sangyeun Cho and **Hyunjin Lee**, "Flip-N-Write: A Simple Deterministic Technique to Improve PRAM Write Performance, Energy and Endurance" *IEEE/ACM International Conference on Microarchitecture (MICRO)*, New York City, New York, December 2009. Acceptance rate ~24.9% (52/209).

- [C.4] Taecheol Oh, **Hyunjin Lee**, Kiyeon Lee, and Sangyeun Cho. “An Analytical Model to Study Optimal Area Breakdown between Cores and Caches in a Chip Multiprocessor” *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pp. 181~186, Tampa, Florida, May 2009.
- [C.5] Sangyeun Cho, Socrates Demetriades, Shayne Evans, Lei Jin, **Hyunjin Lee**, Kiyeon Lee, and Michael Moeng. “TPTS: A Novel Framework for Very Fast Manycore Processor Architecture Simulation,” *IEEE International Conference on Parallel Processing (ICPP)*, pp. 446~453, Portland, Oregon, September 2008. Acceptance rate ~30.8% (81/263).
- [C.6] **Hyunjin Lee**, Sangyeun Cho, and Bruce R. Childers. “Exploring the Interplay of Yield, Area, and Performance in Processor Caches,” *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, pp. 216~223, Lake Tahoe, CA, October 2007.
- [C.7] **Hyunjin Lee**, Sangyeun Cho, and Bruce R. Childers. “Performance of Graceful Degradation for Cache Faults,” *Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pp. 409~415, Porto Alegre, Brazil, May 2007.

#### Refereed Workshop Publications

- [W.1] Lei Jin, **Hyunjin Lee**, and Sangyeun Cho. “Flexible Page-Level Data Mapping to Cache Slices in Multicore Processors,” *Proceedings of the ACM Workshop on Memory Systems Performance and Correctness (MSPC)*, during the *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, San Jose, CA, October 2006.

#### Refereed Poster Publications

- [P.1] **Hyunjin Lee**. “Fault and Yield Aware On-chip Memory Design and Management,” *13th ACM/SIGDA Ph.D Forum at Design Automation Conference (DAC)*, Anaheim, CA, June 2010.

#### INVITED TALKS

- “CloudCache: A Yield and Performance Aware Terascale Adaptive Memory System”
- IBM Research-Austin, Austin, TX, November 2010
- “StimulusCache: Boosting Performance of Chip Multiprocessors with Excess Cache”
- Boeing Research and Technology, Bellevue, WA, October 2010
  - Inter-University Semiconductor Research Center (ISRC), Seoul National University (SNU), Seoul, Korea, January 2010
  - CALCM, Carnegie Mellon University (CMU), Pittsburgh, PA, December 2009
- “Two Techniques for the Yield, Performance, and Reliability Aware Memory Hierarchy Design”
- CS Department, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, February 2010
- “High Speed Processor Simulation Methodology and Its Research Applications”
- Suzhou Institute for Advanced Study (SIAS), University of Science and Technology of China (USTC), Suzhou, China, January 2010

#### REVIEWER

IEEE Transactions on Computers (TC), 2010

IEEE Transactions on Parallel and Distributed Systems (TPDS), 2010

The Fifteenth International Conference on Parallel and Distributed Systems (ICPADS'09)

11<sup>th</sup> & 12<sup>th</sup> Asia-Pacific Computer Systems Architecture Conference (ACSAC 2006, 2007)

**HONORS AND AWARDS**

A. Richard Newton Graduate Scholarship  
*The 45<sup>th</sup> design Automation Conference (DAC) 2008*

3<sup>rd</sup> Place, Hyunjin Lee, “An Extended Motion Estimation Algorithm Based on Discrete Cosine Transform”  
*5<sup>th</sup> HumanTech Thesis Prize, Samsung Electronics, February 1999*

Best Award (2<sup>nd</sup> place), Hyunjin Lee “Enhanced MPEG-2 Motion Estimation Technique”  
*National Thesis Competition for University Student, Ministry of Education, Korea, December 1998*

**REFERENCES**

Sangyeun Cho  
Associate Professor  
University of Pittsburgh  
[cho@cs.pitt.edu](mailto:cho@cs.pitt.edu)

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Associate Professor  
University of Pittsburgh  
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