

# Call for Papers

*IEEE Micro* Special Issue:

## Interaction of Computer Architecture and Operating Systems in the Many-core Era

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### GUEST EDITORS

Sangyeun Cho (cho@cs.pitt.edu), University of Pittsburgh  
Tao Li (taoli@ece.ufl.edu), University of Florida  
Onur Mutlu (onur@microsoft.com), Microsoft Research

### OVERVIEW

Practices and conventions in architecting and designing a microprocessor are undergoing dramatic changes. Squeezing performance from a single, fast, and large core has become a difficult proposition, while incorporating multiple processor cores on a silicon die is relatively effortless thanks to the continuing advances in process technology. Major microprocessor vendors are currently marketing multicore processors, carrying two to eight cores and supporting up to a few dozens of threads simultaneously. Doubling the number of cores in a processor chip with each process technology generation is now conventional wisdom, and the era of “many-core” processors is around the corner.

While implementing microprocessors with many processing cores (and therefore huge potential for greatly escalating user-perceivable performance) is certainly not infeasible, efficiently harnessing processor cores’ raw horsepower and intelligently managing a large amount of on-chip resources remain a difficult challenge. In order to achieve high performance-power and performance-area ratios, for instance, multicore processors are beginning to employ heterogeneous processor cores or even specialized function blocks. On-chip network and distributed shared resources (e.g., L2 cache banks) cause non-trivial performance asymmetry and lack of performance guarantees for co-scheduled programs. Various manufacture-time and run-time variability and technology-induced reliability issues pose further complications to operating next-generation many-core processors in a robust and efficient way.

As the Operating System (OS) or system software in general (including hypervisors or virtual machine monitors), is the centerpiece of a computer system managing various platform hardware resources, the breathtaking evolution of the many-core processor architecture will require a fundamental reexamination of mainstream OS/system-software design decisions. In turn, the evolution of many-core processor architecture will be successfully sustained by the new capabilities and features added to the OS, perhaps with support from hardware. Many important processor resource management issues, including support for Quality of Service (QoS) and differentiated services, fault tolerance and faulty resource isolation, power and thermal control, and efficient virtual machine support, will be best dealt with by a combination and/or

cooperation of novel and well-conceived OS/system-software and hardware architecture techniques. Good interaction between the OS/system-software and new many-core architectures will be essential to successful design of highly efficient and effective computer systems.

The purpose of this special issue of the IEEE Micro magazine is to bring readers the latest advances in the interface of the fields of operating systems and computer architecture, with a focus on how the important system software affects the architecture design and vice versa, in order to achieve increasingly involved platform and system design goals. We are soliciting contributions in areas including but not limited to the following:

- Architecture/OS/system-software support for efficient programming, including parallel programming
- Architecture/OS/system-software support for virtualization and virtual machines
- Architecture/OS/system-software support for memory hierarchy management
- Architecture/OS/system-software support for processor management (scheduling and heterogeneity)
- Architecture/OS/system-software support for reliability enhancement
- Architecture/OS/system-software support for low power consumption and efficient management of energy/power consumption
- Architecture/OS/system-software support for system dependability, availability and security
- Architecture/OS/system-software support for input/output processing
- Architecture/OS/system-software support for providing quality of service to applications
- Architecture/OS/system-software support for multithreading, synchronization, and parallelism

#### **SUBMISSION PROCEDURE**

Log onto IEEE CS Manuscript Central at <http://mc.manuscriptcentral.com/cs-ieee>, and submit your manuscript. For questions, please contact the IEEE Micro magazine assistant at [micro-ma@computer.org](mailto:micro-ma@computer.org).

For the manuscript submission, acceptable file formats include Microsoft Word and PDF. Manuscripts should not exceed 5,000 words (with each average-size figure counting as 150 words toward this limit), including references.

Please include all figures and tables, as well as a cover page with author contact information (name, postal address, phone, fax, and e-mail address) and a 200-word abstract. Submitted manuscripts must not have been previously published or currently submitted for publication elsewhere, and all manuscripts must be cleared for publication. Accepted articles will be edited for structure, style, clarity, and readability. For more information, please visit the IEEE Micro Author Center, online at <http://www.computer.org/portal/site/micro>.

#### **IMPORTANT DATES**

- Paper due: January 5, 2008 (there will be no extension)
- Author notification: February 20, 2008
- Final version due: March 13, 2008
- Publication: May/June 2008