Simultaneous Communication and Processor Voltage Scaling for Dynamic and Leakage Energy Reduction in Time-Constrained Systems

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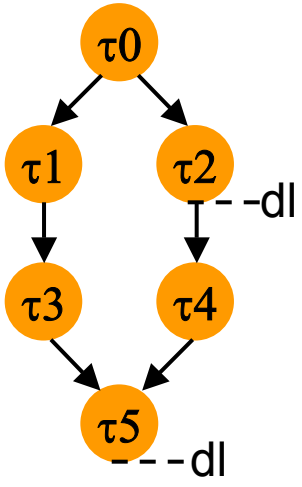
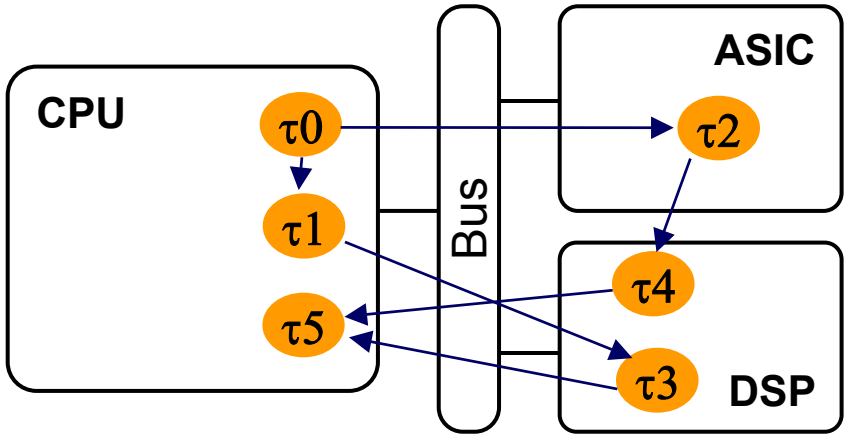
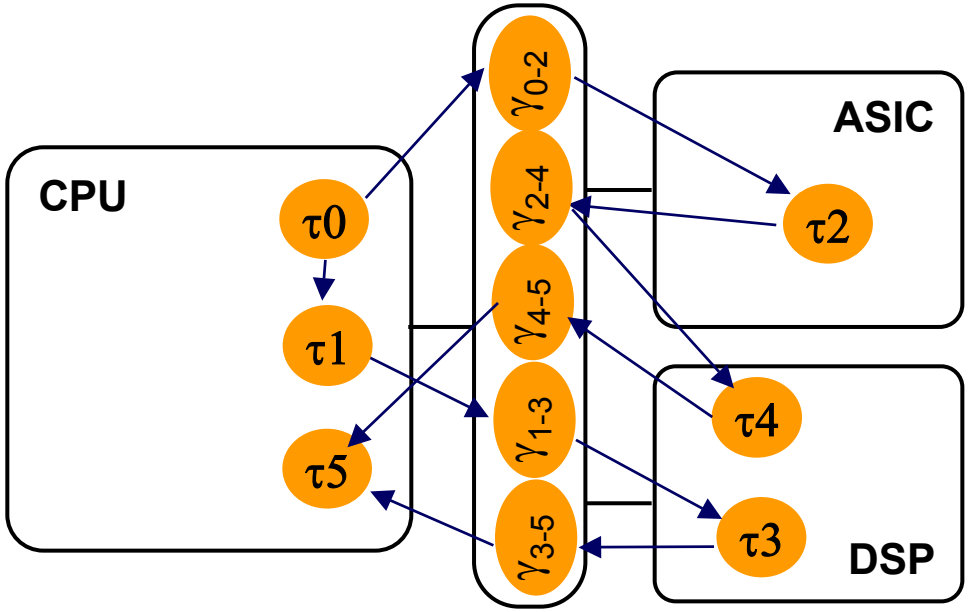
Introduction



Application model

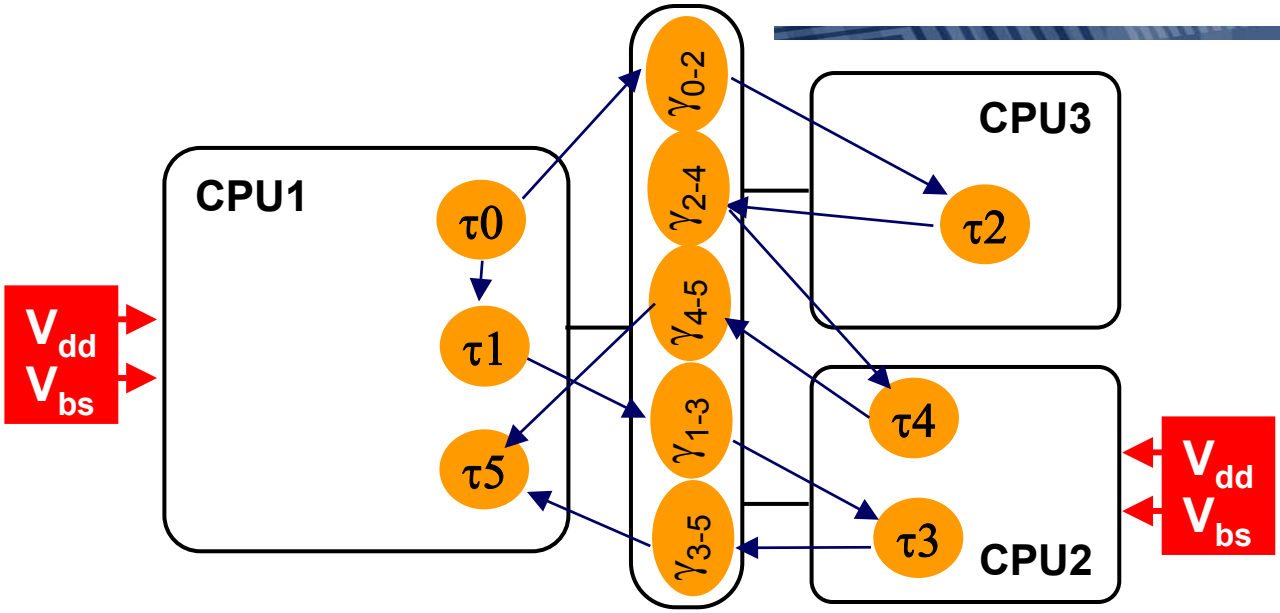


Architecture model

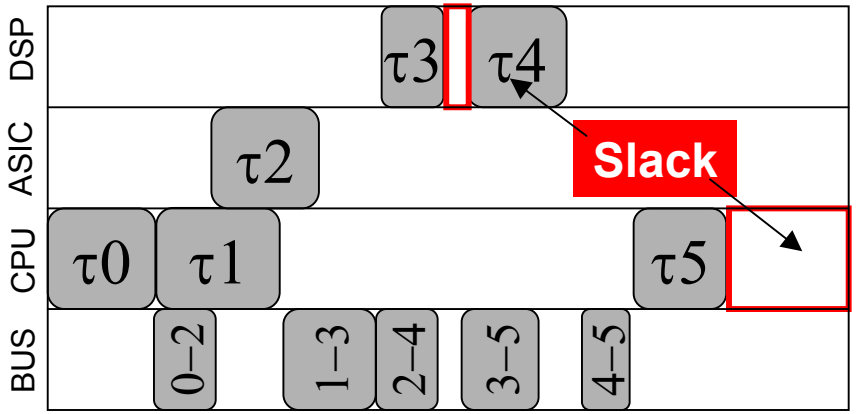


Architecture model with communication

Introduction



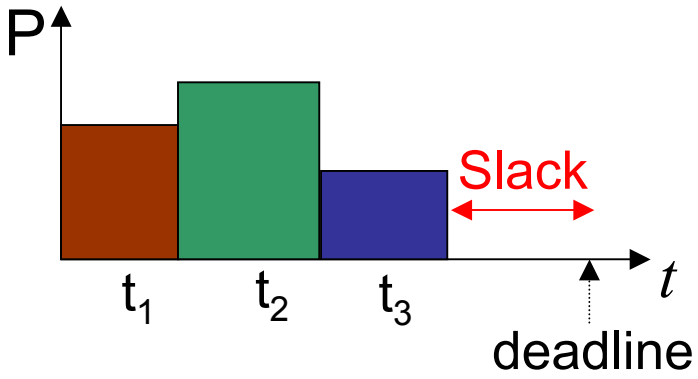
Architecture & Mapping

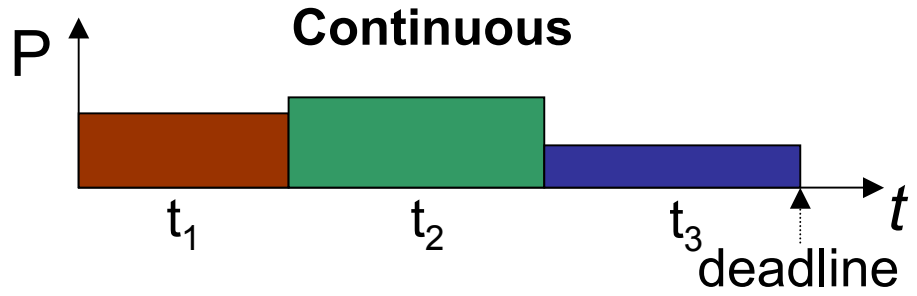


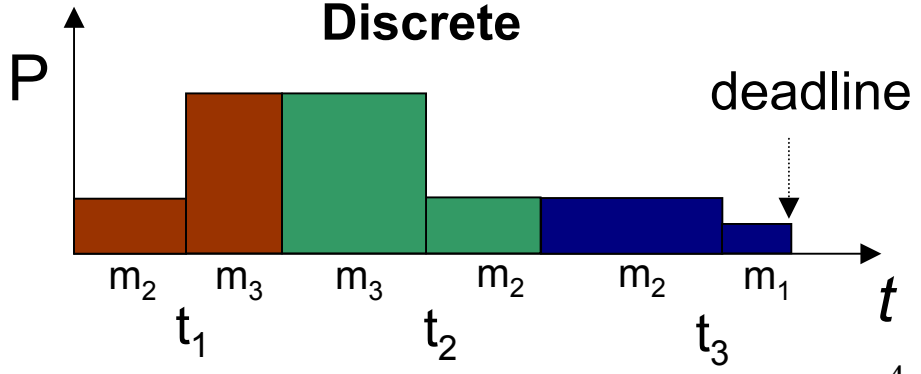
Schedule

Dynamic Voltage Selection

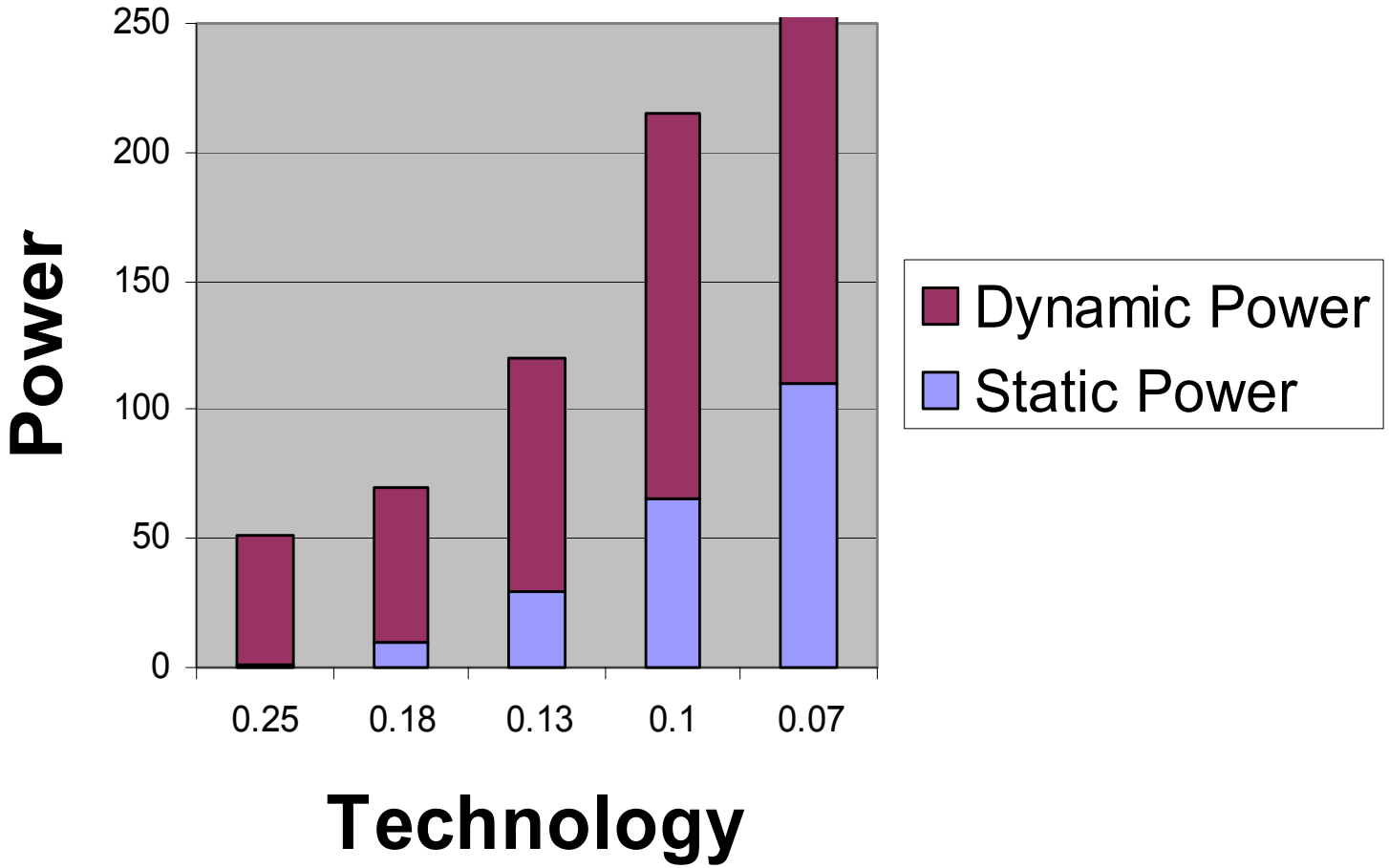
- The processors can work over a **continuous range** or a **discrete set** of execution modes (voltage pairs)



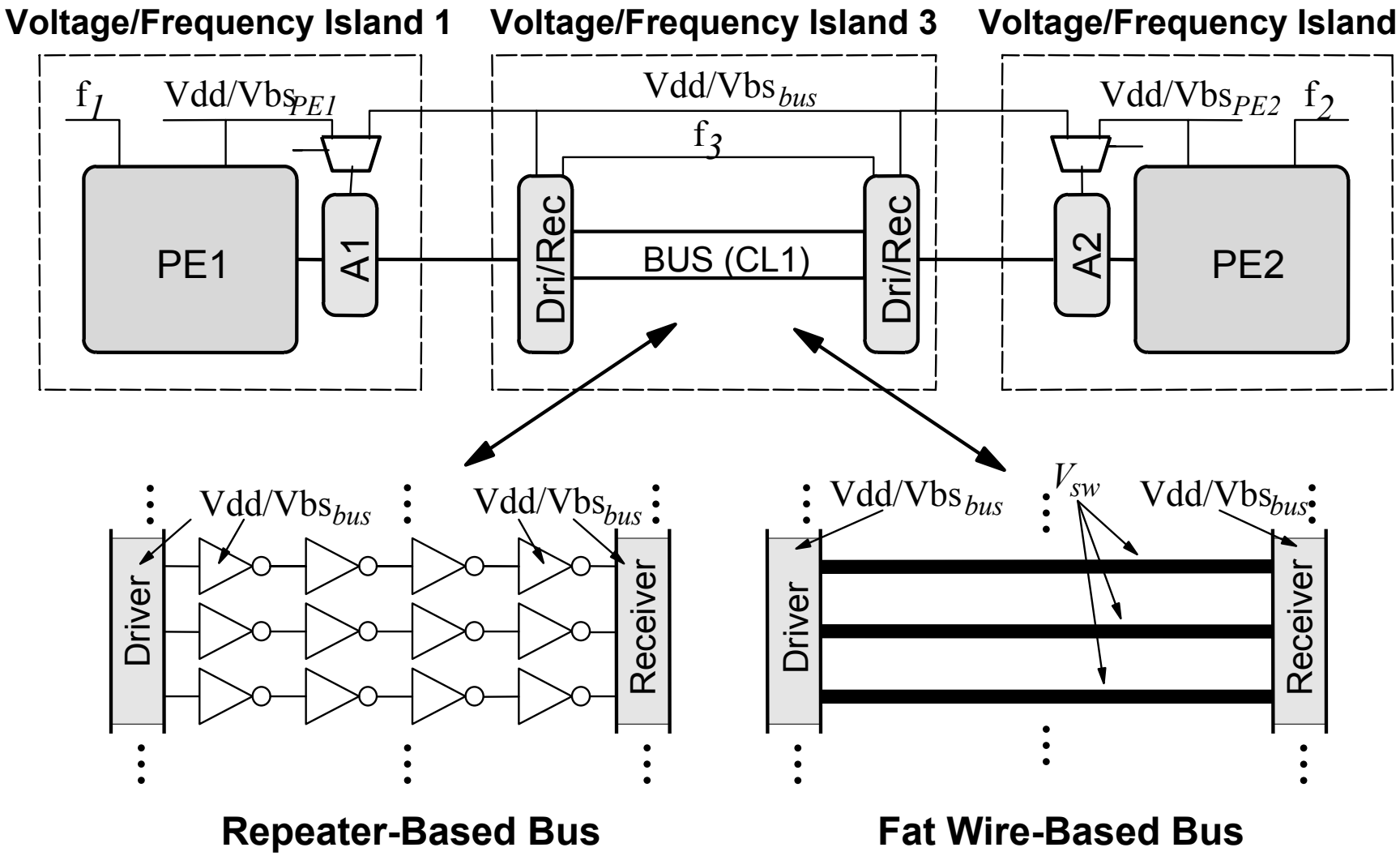




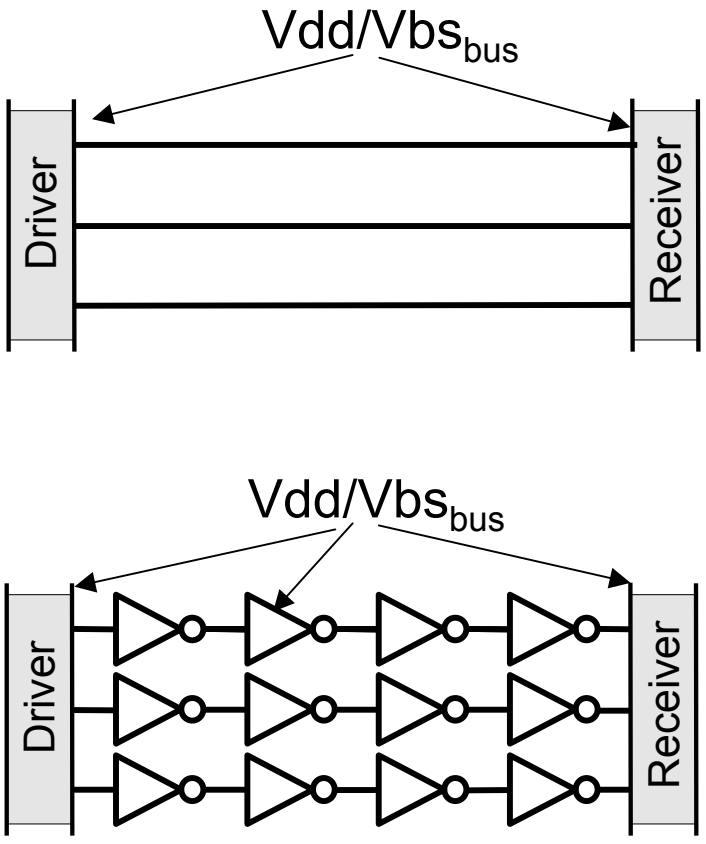
Energy Distribution



Communication Model



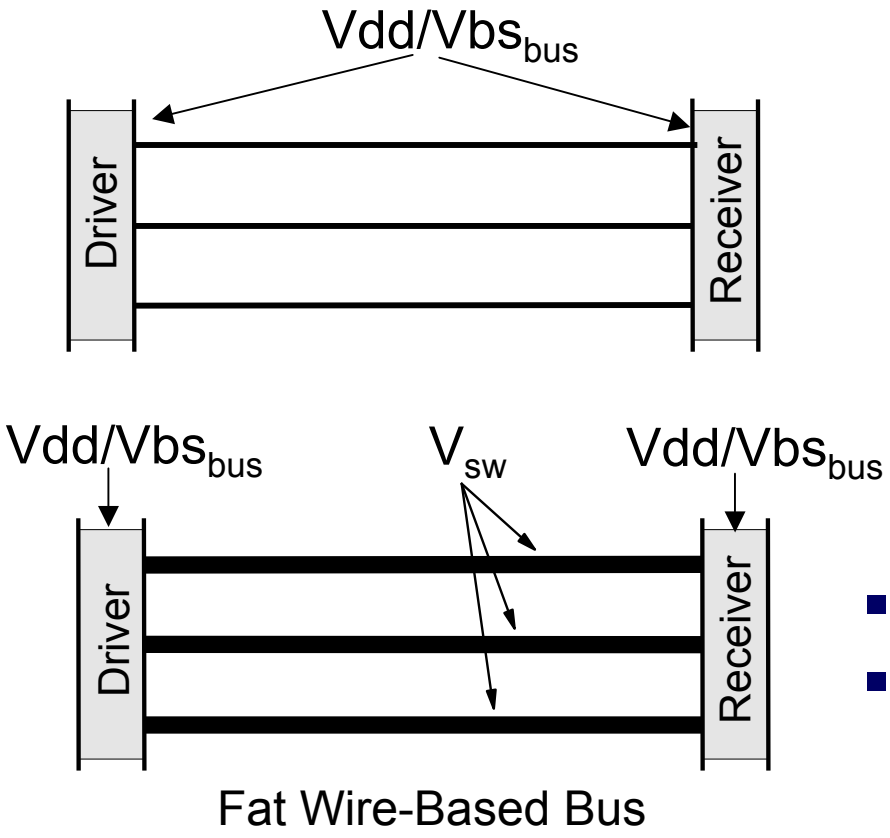
Repeater-Based Bus



Repeater-Based Bus

- Repeaters speed-up the wires
- The number of repeaters can be optimized for speed, power and/or area
- Power hungry
- Voltage scaling of the repeater based bus

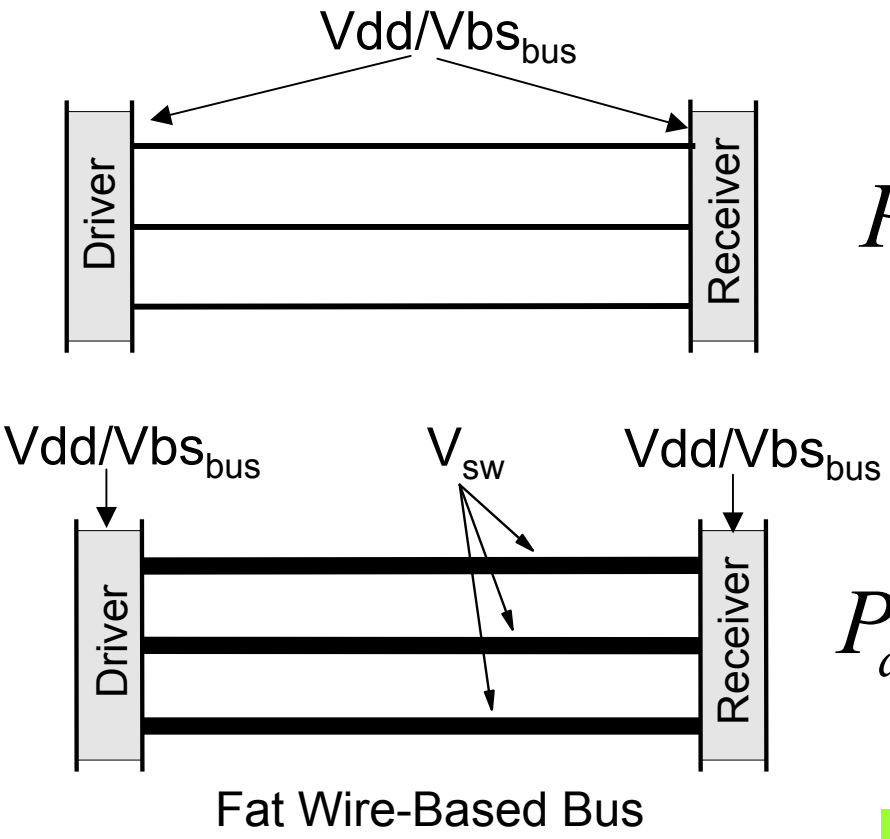
Fat Wire-Based Bus



Fat Wire-Based Bus

- High speed
- Only possible with short wires

Fat Wire-Based Bus



Fat Wire-Based Bus

$$P_{dri} = sw \cdot f_{bus} \cdot C_{wire} \cdot V_{bus}^2$$

$$C_{fat\_wire} >> C_{wire}$$

$$P_{dri} = sw \cdot f_{bus} \cdot C_{fat\_wire} \cdot V_{bus}^2$$

Use a low voltage swing

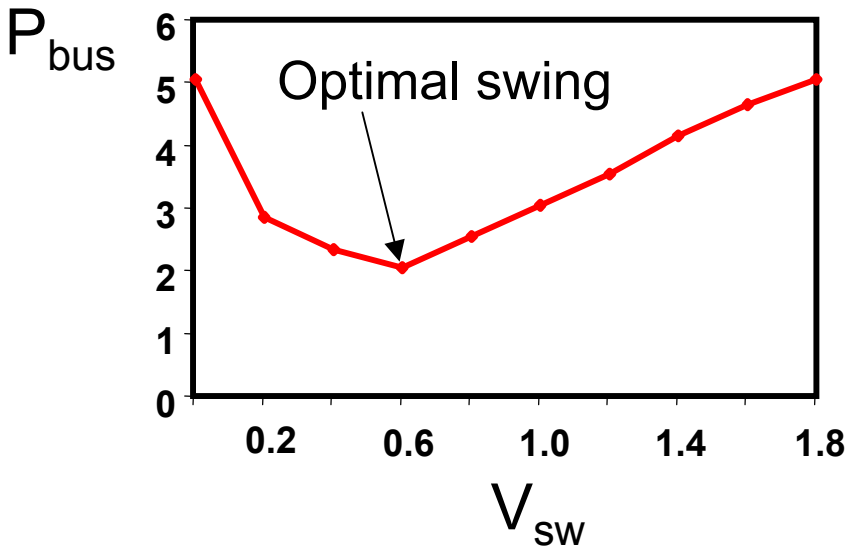
$$P_{dri} = sw \cdot f_{bus} \cdot C_{fat\_wire} \cdot V_{bus} \cdot V_{sw}$$

Optimum Swing on a Fat Wire-Based Bus

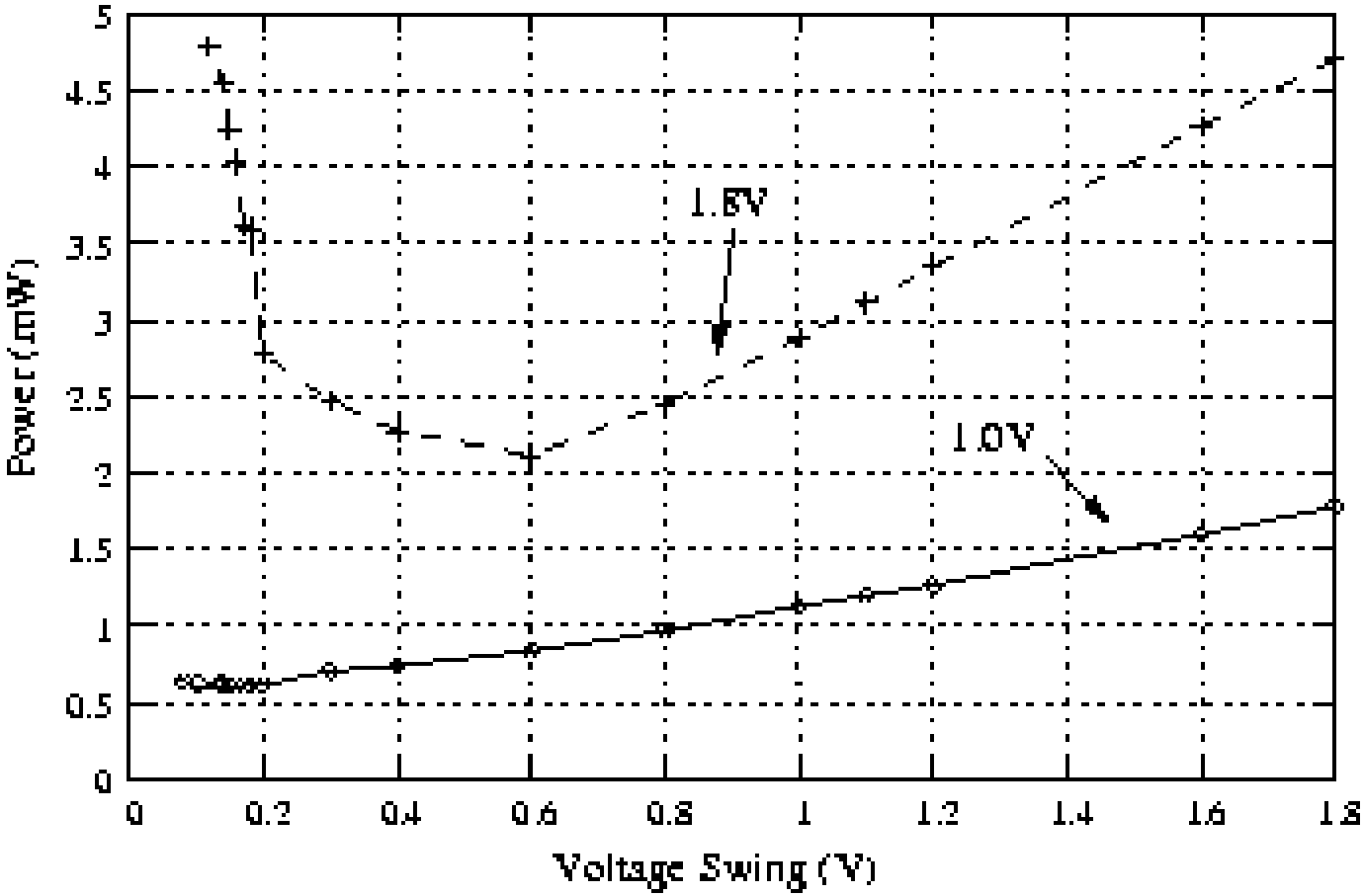
$$P_{bus} = P_{dri} + P_{rec}$$

$$P_{dri} = sw \cdot f_{bus} \cdot C_{fat\_wire} \cdot V_{bus} \cdot V_{sw}$$

$$P_{rec} = sw \cdot f_{bus} \cdot C_{fat\_wire} \cdot V_{bus} \cdot V_{sw}$$



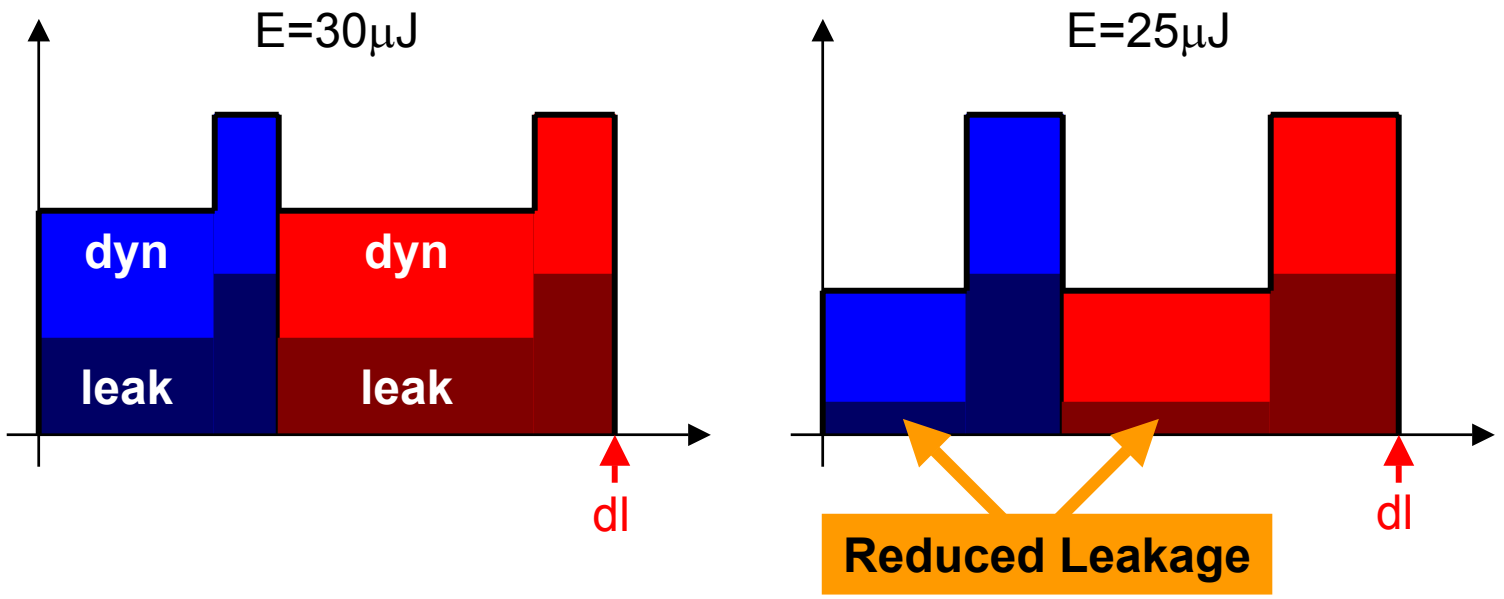
Optimum Swing on Fat Wires



Contributions

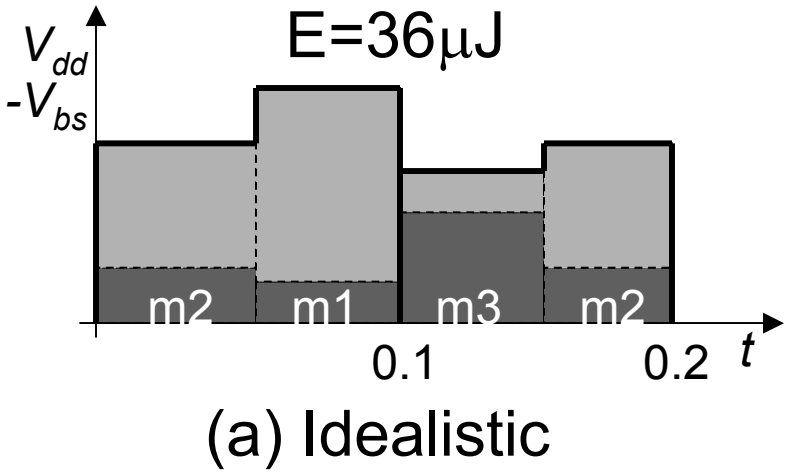
- Consider **supply and body bias** scaling at the system level
- Scaling of processors and buses
- Usage of appropriate models for the communication infrastructure
- Consider transition overheads (delay and energy) during optimization
- Polynomial time optimal algorithms for the continuous voltage scaling
- Heuristic for the discrete voltage selection

Motivation: Supply and Body Bias Scaling

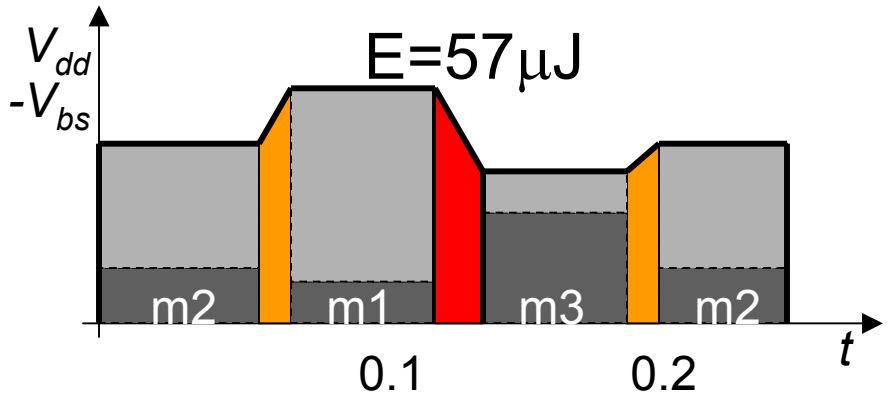


V_{dd} and V_{bs} scaling necessary!

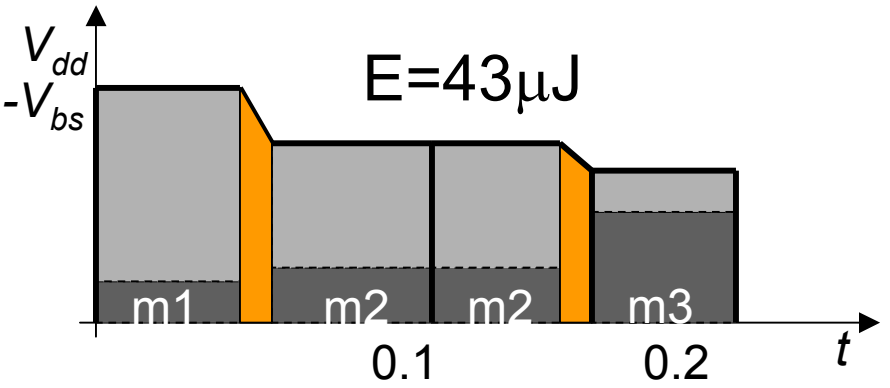
Motivation: Transition Overheads



(a) Idealistic



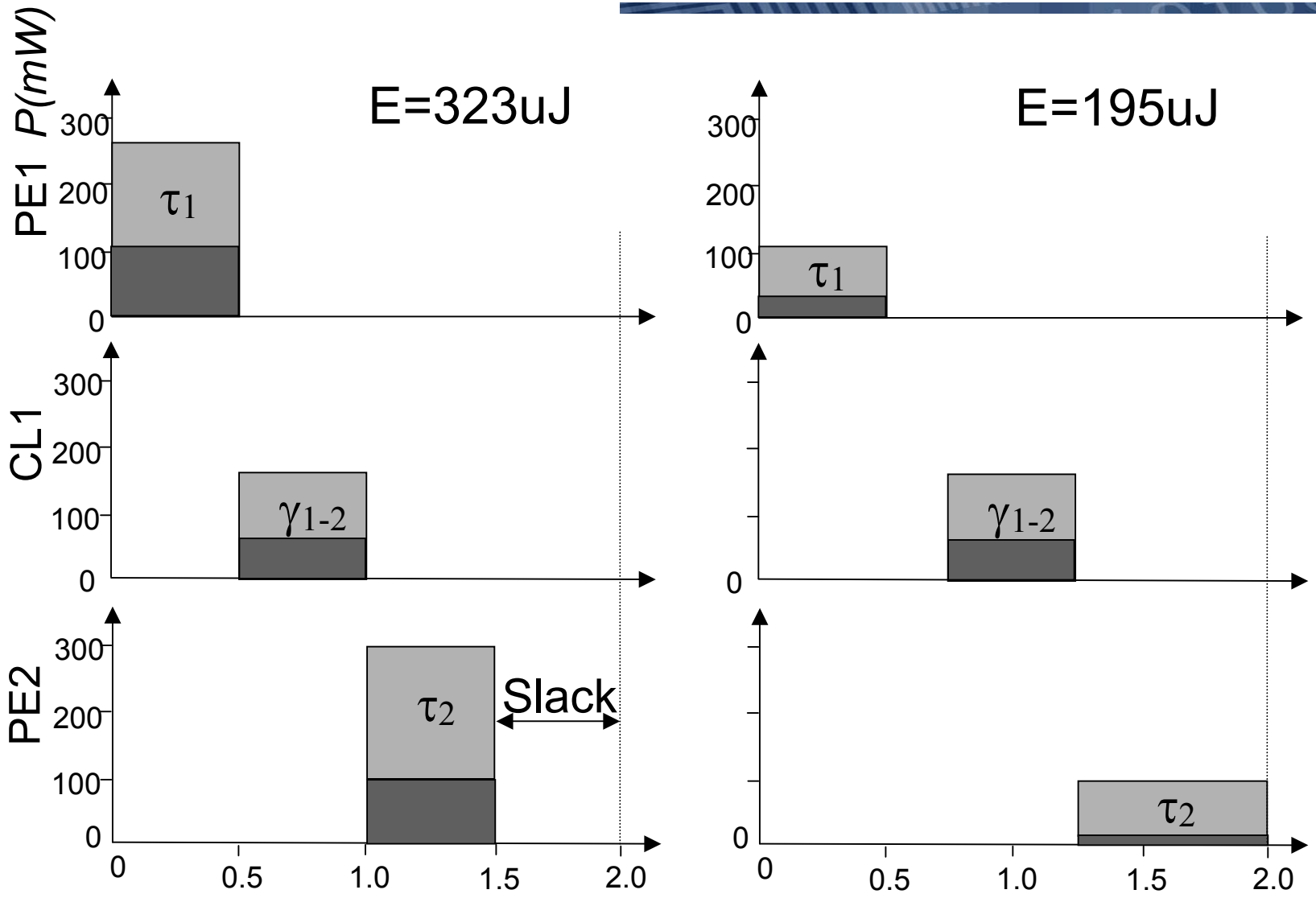
(b) During run-time



(c) Reordered

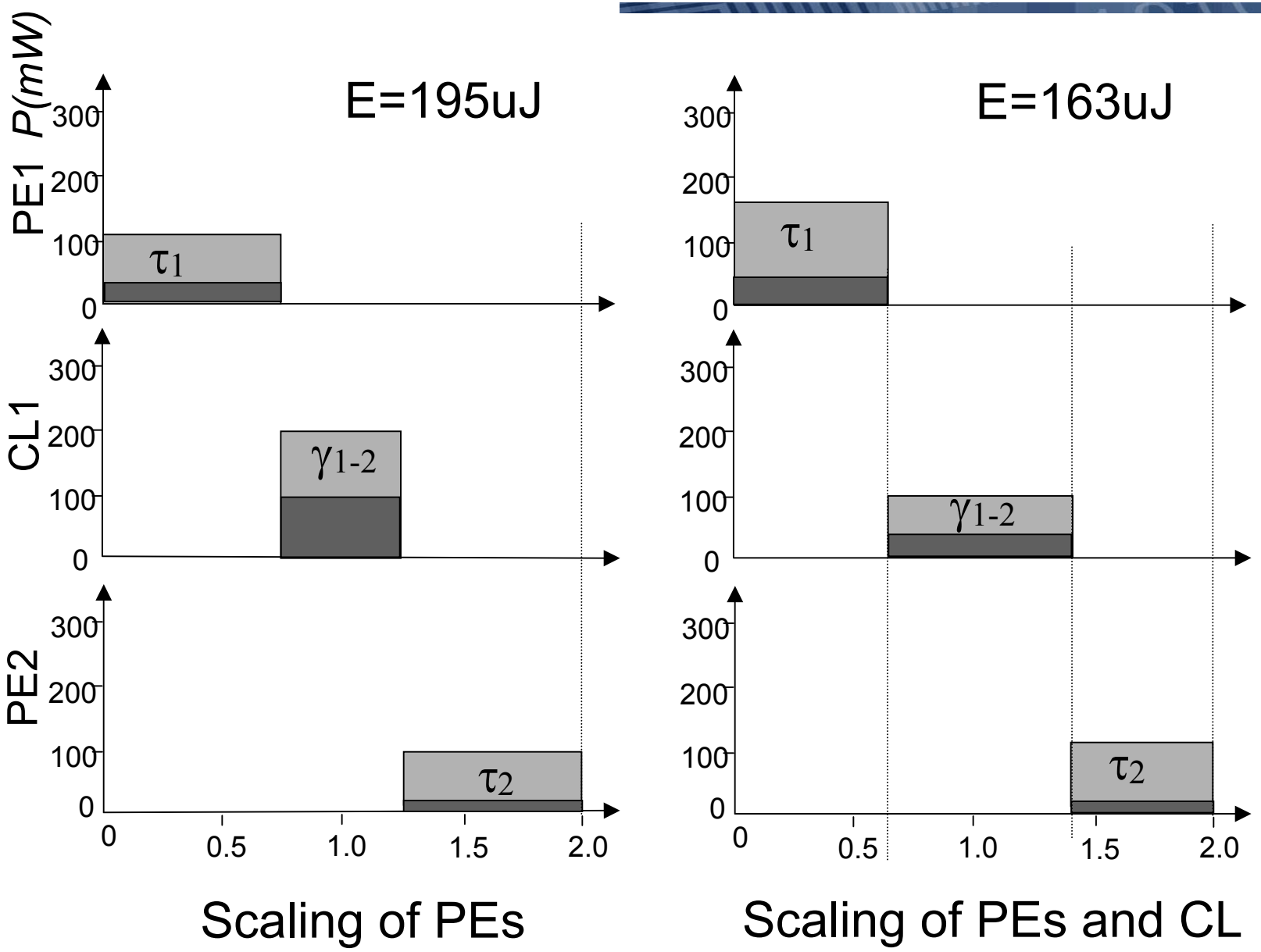
Consider the transition overheads during optimization

Motivation: Bus Scaling



Schedule without voltage scaling Scaling of PEs

Motivation: Bus Scaling



Scaling of PEs

Scaling of PEs and CL

Continuous Voltage Scaling

- Can be formulated as a ***convex nonlinear problem***

Minimize: Dynamic + Leakage Energy

Such that:
- *precedence constrains*
- *deadlines*
- *scheduling constraints*

- Polynomial time solvable with an *arbitrary good* precision

Transition Overheads

- Can be formulated as a ***convex nonlinear problem***

Minimize: Dynamic + Leakage Energy + ***OH Energy***

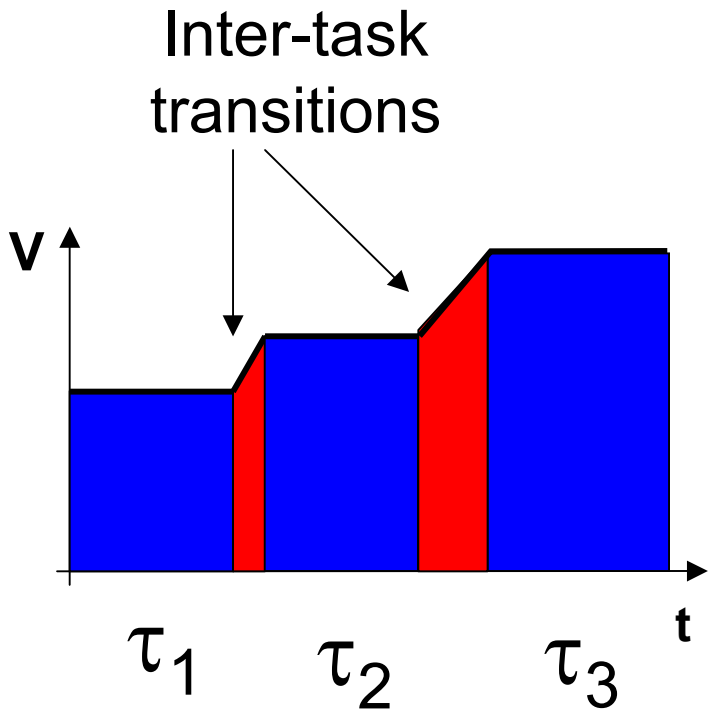
Such that:
- *precedence constrains*
- *scheduling constraints*
- *deadlines*
- ***including timing overheads***

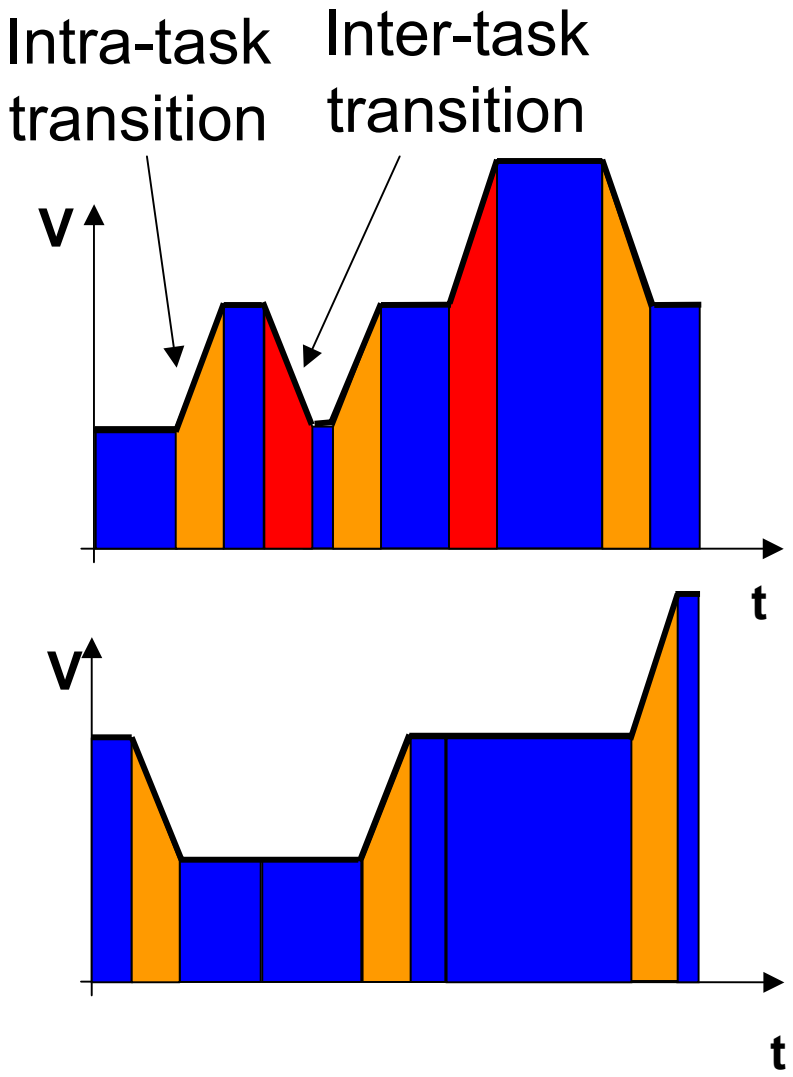
- The overheads (time, energy) are expressed in terms of V_{dd} and V_{bs} variations

Discrete Voltage Selection

- NP strongly hard (no pseudopolynomial algorithm exists)
- MILP formulation for the optimal solution
- A polynomial time heuristic for solving the discrete problem efficiently

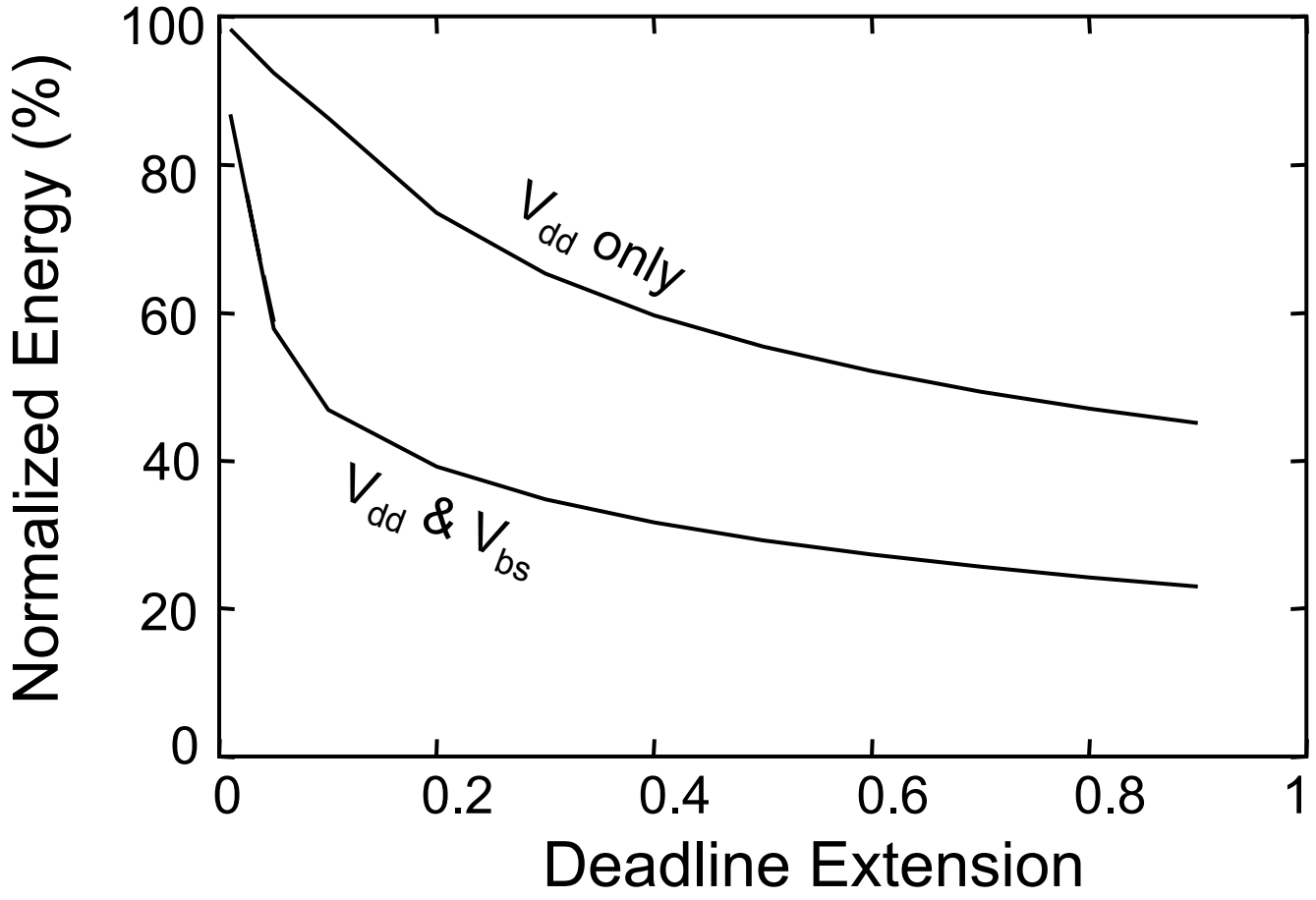
VS Heuristic



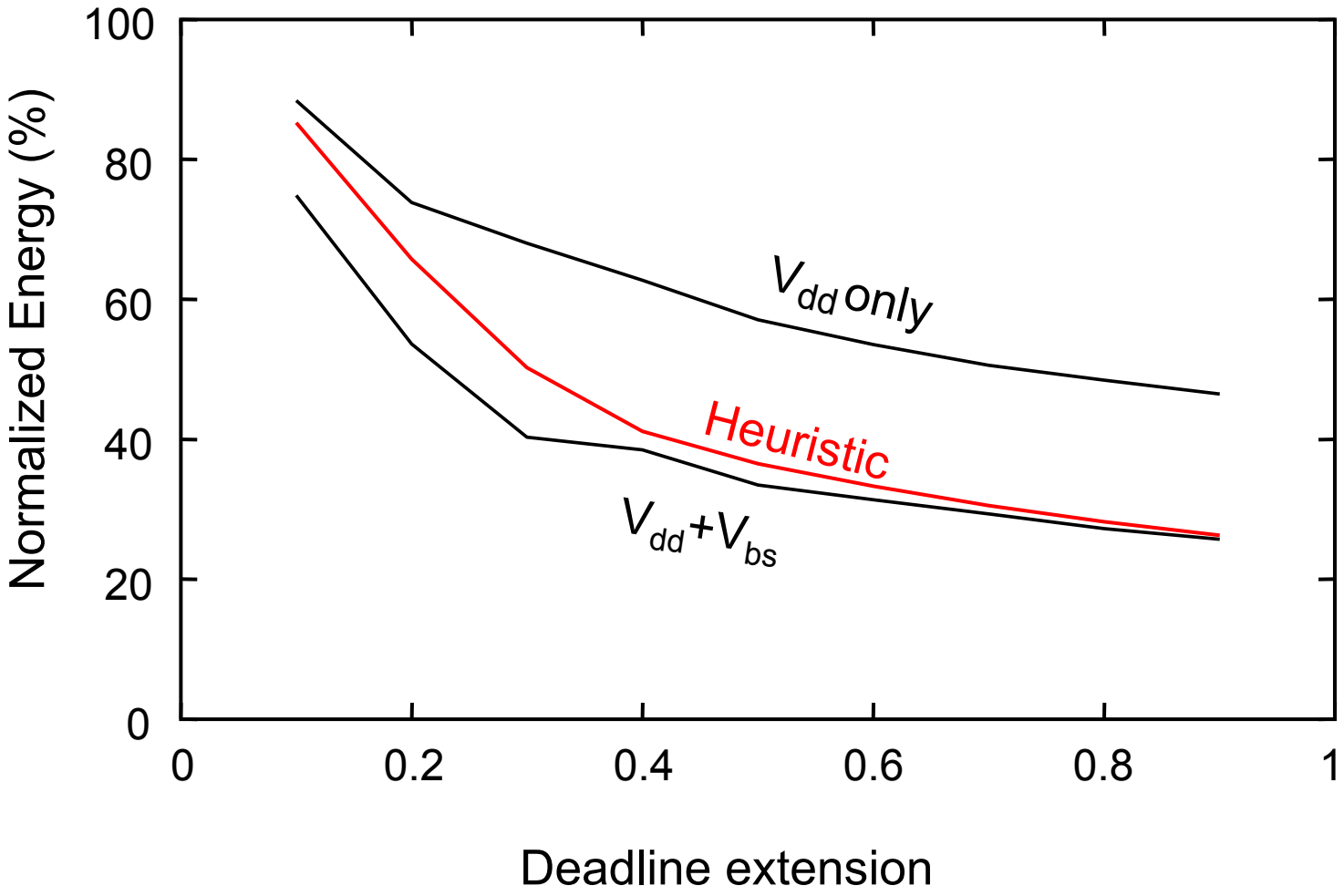


Continous Solution => Discrete Solution

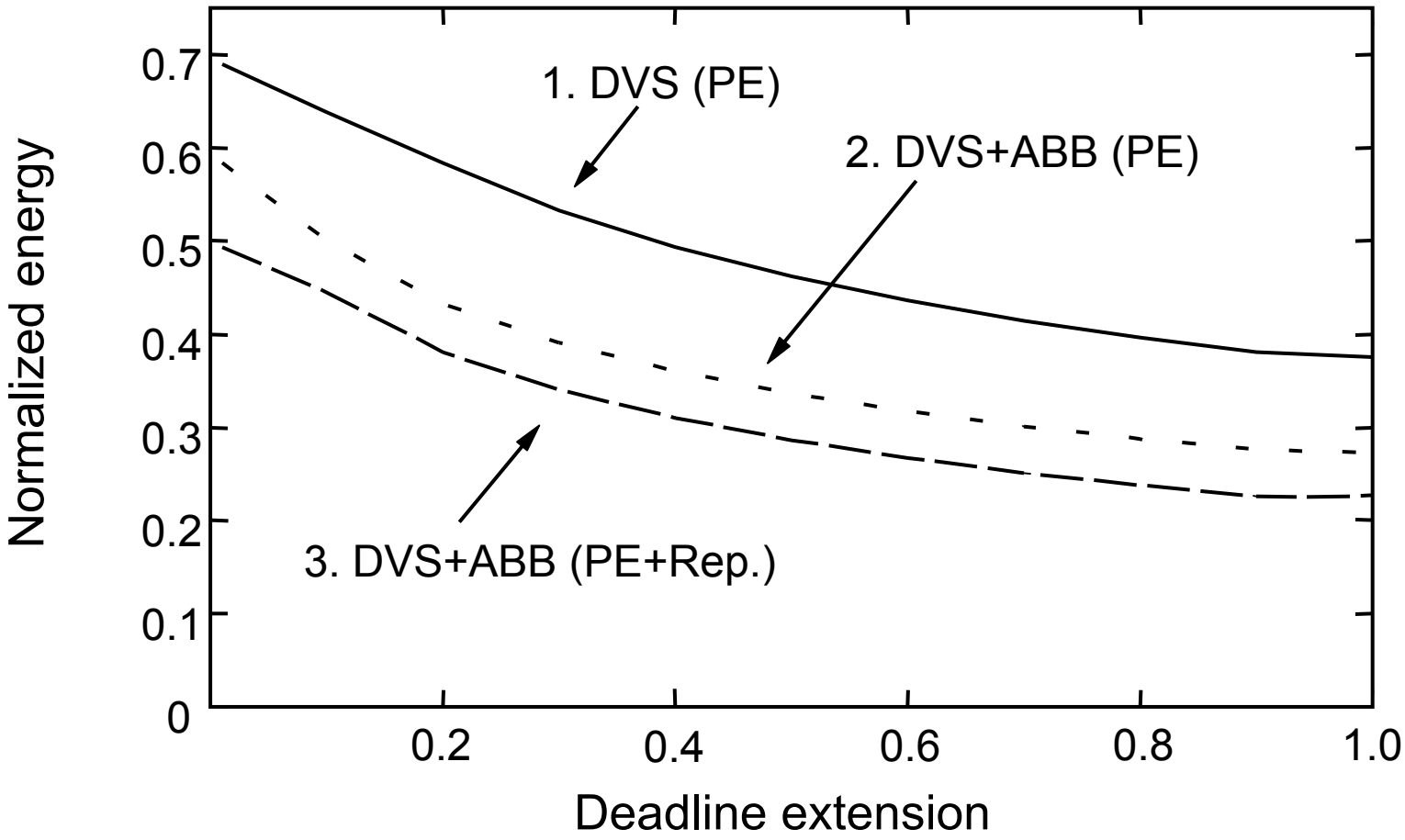
Experimental Results: Continuous VS



Experimental Results: Discrete VS

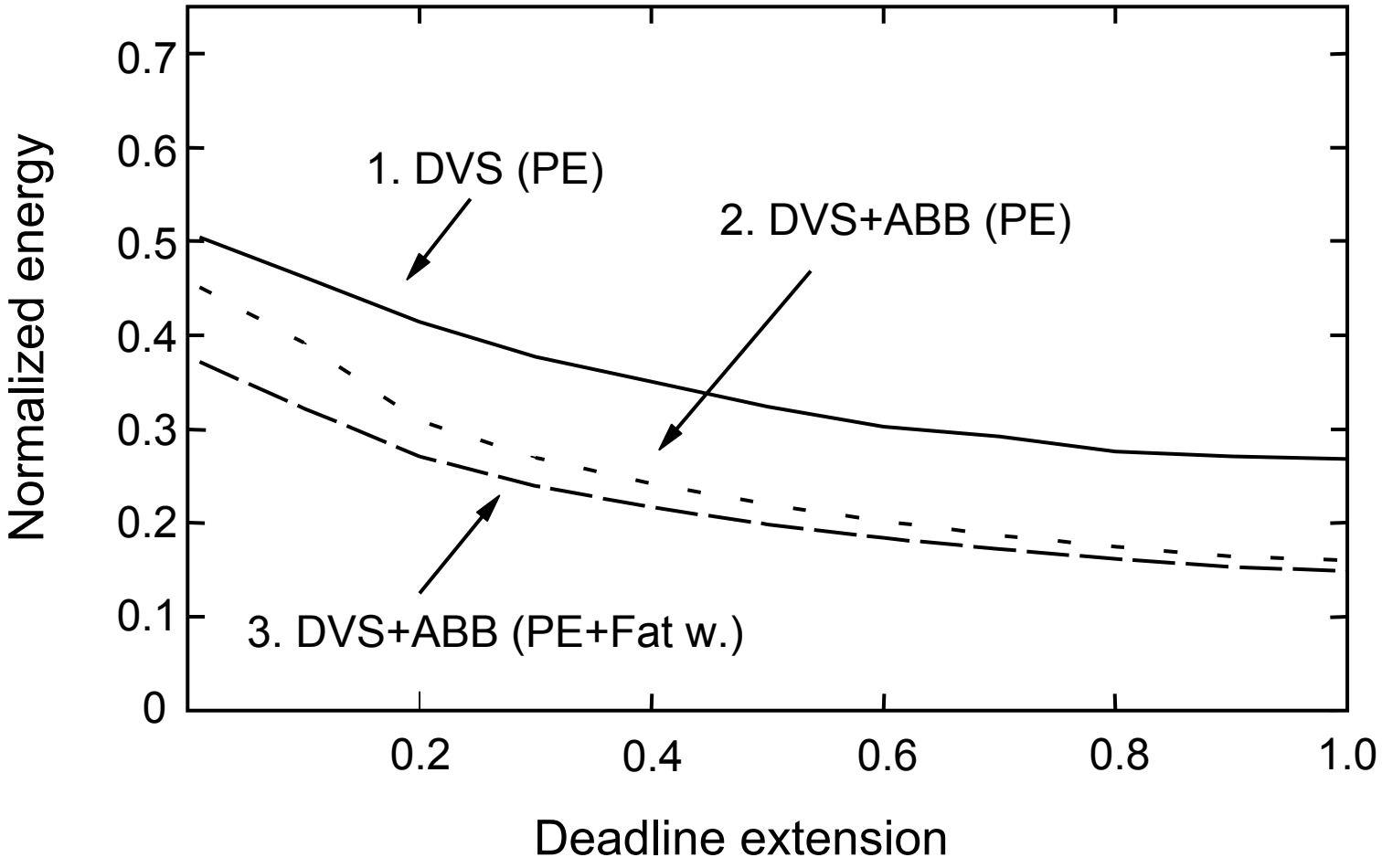


Experimental Results: Bus Scaling(1)



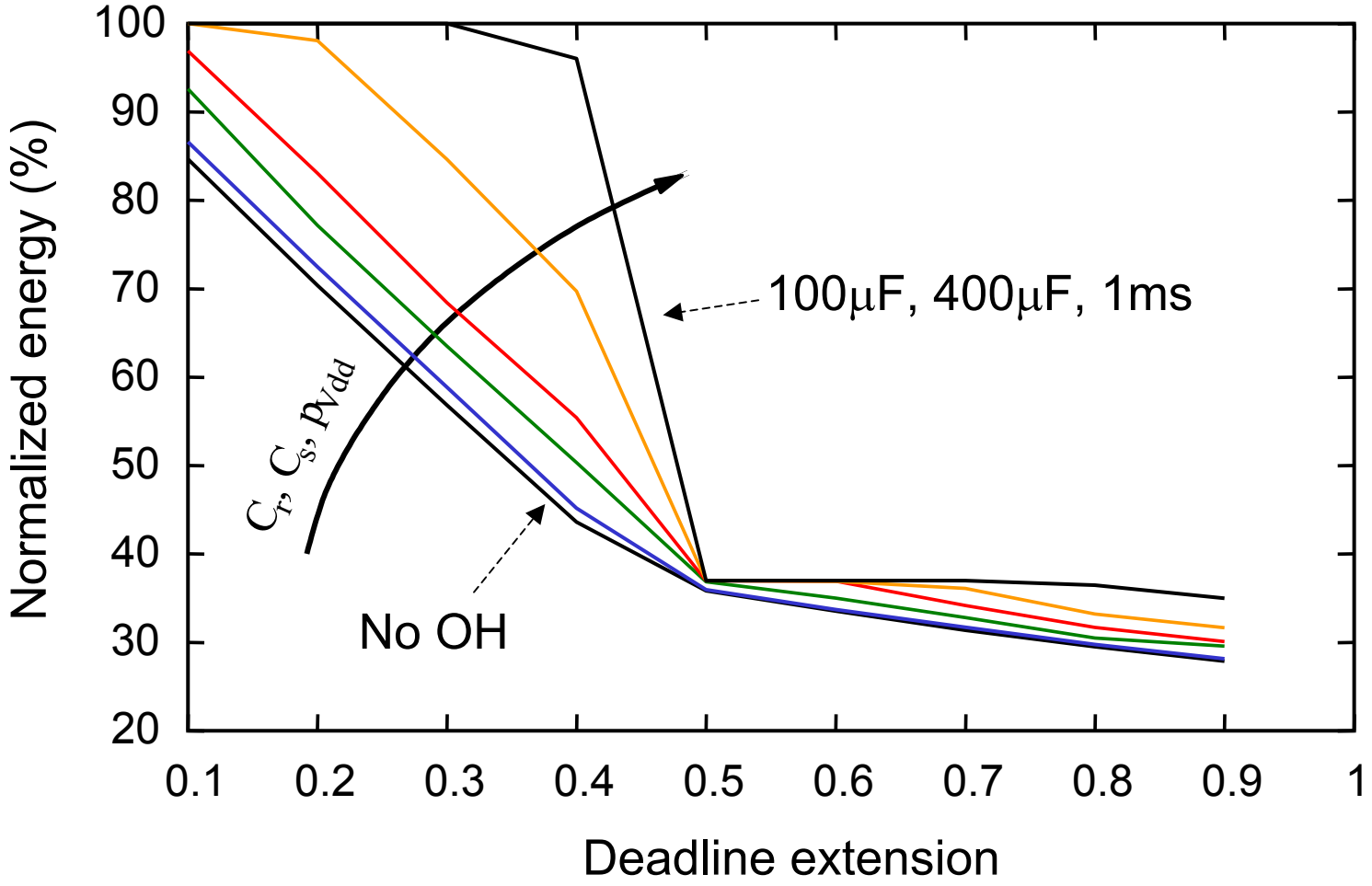
(1) Energy dissipation of a repeater-based system

Experimental Results: Bus Scaling(2)



(b) Energy dissipation of a fat wire-based system

Experimental Results: Overheads



Conclusions

- Supply and body bias scaling at the system level
- Consider transition overheads (delay and energy)
- Continuous voltage scaling – polynomial time optimal solution
- Discrete voltage selection is strogly NP hard
- Heuristic for the discrete voltage scaling
- Experiments with synthetic task graphs and a real-life application

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